

ARRAY-BASED PLANAR NANOWIRE HIGH ELECTRON
MOBILITY TRANSISTOR

BY

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DISSERTATION

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ABSTRACT

III-V semiconductor nanowire (NW) field-effect transistors (FETs) are strong candidates for future low-power digital/RF IC. Bottom-up grown NWs via the vapor-liquid-solid (VLS) mechanism are of particular interest for NW-FET application because the as-grown 3D NW structures require no lithography or chemical etching to define. However, fabricating bottom-up NW-FETs and circuits in wafer-scale is still in question. The main challenges include: controllability of NW position, uniformity of NW electrical property, and compatibility with planar processing.

In this thesis research, a bottom-up planar-NW high electron mobility transistor (HEMT) technology was developed to overcome the above challenges. Uniform and scalable electrical properties were demonstrated by prototype planar NW HEMTs with multiple 250 nm diameter planar NWs in the channels. Through growth optimization and using a two-temperature-step growth method, defect-free planar GaAs NWs with width as small as 35 nm and tapering factor of better than 1:1000 were achieved. With the down-scaled planar GaAs NWs serving as the channel, a monolithic grown barrier-all-around planar NW HEMT was made with peak $G_{m-ext} = 550 \mu S/\mu m$ and $I_{d-max} = 435 \mu A/\mu m$, surpassing its thin-film counterparts. Growth effort with top-down patterned metal catalysts enabled the realization of precisely positioned planar NW arrays in wafer-scale. Having the NW arrays as the channels, planar NW array-based HEMTs were for the first time demonstrated with excellent DC/RF performances: $I_{on}/I_{off} \sim 10^4$, $SS \sim 102$ mV/dec, $DIBL \sim 151$ mV/V and $f_T / f_{max} \sim 33/75$ GHz. To our knowledge, the DC/RF performances achieved here are the best among the nanoscale devices with VLS NWs, carbon nanotubes, or 2D sheets aligned in-plane with the substrate.

To my mother and father

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CHAPTER 1 – INTRODUCTION

For vapor-liquid-solid (VLS) grown NWs, good control of the NW location, growth direction and doping is the key to make this bottom-up nanotechnology feasible for practical large-scale application. In this chapter, these critical aspects of VLS III-V NWs are reviewed. The limitations and challenges of the current VLS technology are also discussed.

1.1 VLS growth mechanism

VLS growth method has been widely used for the synthesis of semiconductor nanowires (NWs) [1]. In a typical VLS NW growth, metal seeds are used to form alloy droplets (liquid) with the growth materials supplied from the gas environment (vapor). As the growth materials accumulate and saturate in the alloy droplets, NWs (solid) composed by the growth materials would precipitate out along certain crystal directions in which the growth system has the lowest total free energy. Generally, the total free energy in VLS NW growth is determined by the surface free energy of the interface between the NW and the alloy droplet. The (111) and (111)B facets have been found to have the lowest surface free energy for group IV elemental and III-V compound semiconductors, respectively [2, 3]. Therefore, the preferred NW growth directions are $\langle 111 \rangle$ for diamond IV NWs [1], $\langle 111 \rangle$ B for zinc-blende (ZB) III-V NWs [4, 5] and $\langle 0001 \rangle$ for wurtzite (WZ) III-V NWs [6-9]. The diameters of VLS NWs are usually comparable to the sizes of the metal seeds. Figure 1.1 illustrates the VLS growth mechanism via an example of growing $\langle 111 \rangle$ Si NWs on (111) Si substrates.

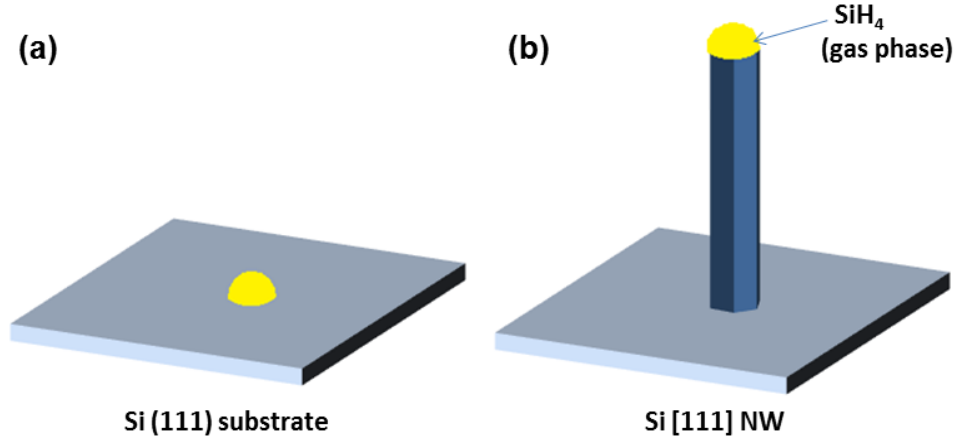


Figure 1.1: VLS growth of $\langle 111 \rangle$ Si NWs on (111) Si substrates. (a) Metal (Au) seeds are deposited and annealed above the Au-Si eutectic temperature prior to the VLS growth. (b) Si atoms from the vapor phase SiH_4 incorporate into Au-Si alloy droplets and precipitate $\langle 111 \rangle$ Si NWs.

1.2 III-V NW

1.2.1 Vertical III-V NW

For the ease of large-scale integration, vertical NWs rather than slanted NWs are preferable. Because of the directional growth property of VLS NWs, growing $\langle 111 \rangle$ B ZB or $\langle 0001 \rangle$ WZ III-V NWs on (111) B III-V substrates is a natural choice to make vertical III-V NWs. In order to have high vertical NW yield, growth conditions such as the growth temperature, reactor pressure, precursor molar flow and the group V to III molar flow ratio (V/III ratio) need to be optimized. In the growth of GaAs NWs on (111) B GaAs substrates, high V/III ratio (AsH_3 to trimethylgallium) of > 90 was found to induce kinking in NWs which would alter the growth directions from the expected $\langle 111 \rangle$ B to non- $\langle 111 \rangle$ B directions [10]. This could possibly be due to the formation of stable As trimmers on the (111) B growth front which changed the surface free energy [11].

If the (111)B III-V substrates are of materials that have different lattice constants as the NWs, there would be misfit strain at the interfaces between the III-V NWs and the substrates. The misfit strain can be coherently released through lateral relaxation if the diameters of the NWs are below certain critical diameters [12]. Under such circumstances, NWs tend to grow along the $\langle 111 \rangle_B$ directions [13]. When the diameters of NWs are beyond the critical diameters, random planar defects such as dislocations and stacking faults would be generated in the NWs and perturb the NW growth directions into non- $\langle 111 \rangle_B$ directions [13, 14].

Besides the lattice-mismatch problem [13, 15], growing vertical III-V NWs on (111) IV substrates is more difficult because all $\langle 111 \rangle$ directions above the substrates are equivalent. III-V NWs grown along all four equivalent $\langle 111 \rangle$ directions on (111) Ge and Si substrates were observed [16, 17]. It has been noted that the degree of misfit between III-V NWs and the IV substrates determines the tendency of III-V NWs to grow in the vertical or the non-vertical $\langle 111 \rangle$ direction [5, 18]. For III-V NWs that have large lattice-mismatch with the elemental substrates, such as InP on Si (8.1%) [17, 19] and InAs on Si (11.6%) [17], NWs tend to grow in non-vertical $\langle 111 \rangle$ directions. For III-V NWs that have moderate lattice-mismatch with the substrates, such as InP on Ge (3.7%) [16] and GaAs on Si (4.1%) [17, 19-21], NWs grow in all equivalent $\langle 111 \rangle$ directions. More importantly, III-V NWs that have small lattice-mismatch with the substrates tend to grow vertically on the substrates, such as GaP on Si (0.4%) [17, 19] and GaAs on Ge (0.1%) [18].

1.2.2 Planar III-V NW

It was noticed by many research groups that a few $\langle 110 \rangle$ GaAs planar NWs exist in the growth of $\langle 111 \rangle_B$ GaAs NWs on (100) GaAs substrates [22-24]. These $\langle 110 \rangle$ GaAs NWs grow

in the plane of the substrate surfaces and are readily compatible with current planar processing technology. Since the in-plane planar NWs on common low-index substrates are not along the energy favorable $\langle 111 \rangle_B$ and $\langle 0001 \rangle$ directions, unconventional growth techniques are needed to increase the planar NW yield.

Controlled growth of stacking-fault-free $\langle 110 \rangle$ GaAs planar NWs on (100) GaAs substrates has been demonstrated with metal–organic chemical vapor epitaxy (MOCVD) reactor through the optimization of the growth temperature and reactor pressure in a wide range of V/III ratio [25]. Under atmospheric reactor pressure, $\langle 111 \rangle_B$ GaAs slanted NWs are the majorities at low growth temperature ($<450^\circ\text{C}$) (Figure 1.2a), whereas $\langle 110 \rangle$ GaAs planar NWs are dominate (Figure 1.2b) at high growth temperature ($>450^\circ\text{C}$) [25]. Figure 1.2c indicates the epitaxial relation between the GaAs planar NW and the substrate. As can also be seen in Figure 1.2c, $\langle 110 \rangle$ GaAs planar NWs have defect-free ZB crystal structure and (111) $_B$ growth fronts (the as shown Au/NW interface was altered a little during reactor cool-down).

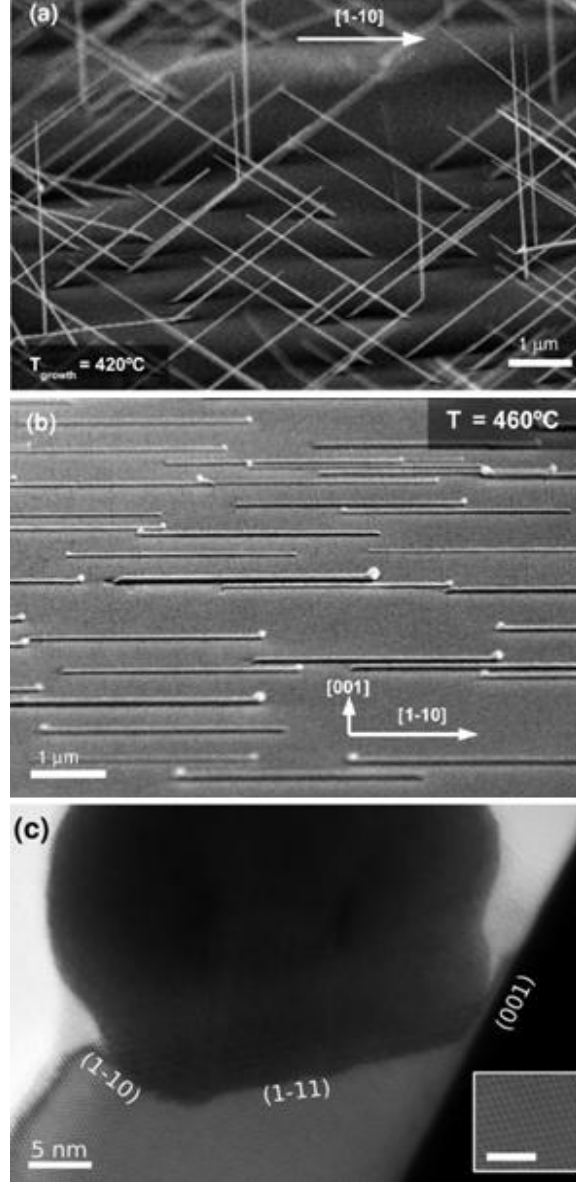


Figure 1.2: GaAs NWs grown under atmospheric pressure on (100) GaAs substrates. (a) At 420°C, $\langle 111 \rangle$ B GaAs slanted NWs are the majority. (b) At 460°C, $\langle 110 \rangle$ GaAs planar NWs dominate. (c) TEM image shows the epitaxial relation between the GaAs planar NW and the substrate. Inset shows that the planar NW has defect-free ZB crystal structure (scale bar is 2.5 nm). Reproduced from Reference [25].

Note in Figure 1.2b that the $\langle 110 \rangle$ GaAs planar NWs grow bi-directionally in $[0-11]$ and $[01-1]$ directions which match with the surface projections of the two equivalent $\langle 111 \rangle$ B directions above the (100) GaAs substrate. Also note that the $\langle 110 \rangle$ GaAs planar NWs have

(111)B growth front (Figure 1.2c); a hypothesis relating the growth directions of planar NWs to the surface projections of $\langle 111 \rangle$ B directions was proposed and verified via planar NW growth on vicinal substrates [26, 27]. Planar NWs of materials other than GaAs have also been demonstrated, such as $\langle 110 \rangle$ $\text{In}_{0.04}\text{Ga}_{0.96}\text{As}$ planar NWs on (311)B GaAs substrate [28], $\langle 110 \rangle$ InAs planar NWs on (100) InAs substrate [29] and $\langle 110 \rangle$ GaAsP planar NWs on (100) GaAs substrate [30]. Although the growth mechanism of planar NWs is still under investigation, good substrate-wetting capability of the compound alloy droplets (metal seeds alloyed with the group III species) is believed to facilitate the planar NW growth [31].

1.2.3 Doping of III-V NW

The doping of VLS NWs is usually done by delivering dopants in vapor phase during the growth of NWs. Following the initial work on the doping of Si NWs [32], VLS III-V NWs doped with p and n types were demonstrated [33]. Because VLS NWs have small sizes and different doping mechanisms with the thin film doping, precise doping control in VLS NWs is challenging [34]. In VLS NW growth, there are two possible paths for dopant incorporation (Figure 1.3), which makes the doping control even more complicated [35]. The first dopant incorporation path is through the VLS mechanism: dopants dissolve in the alloy droplets and then diffuse across the liquid-solid interface to the NW core. The second path is through vapor phase epitaxy (VPE) in which the dopants directly incorporate into the VPE shell around the NW. Obviously, with the unwanted doping via VPE, the doping profile in NWs' radial directions can hardly be uniform. Even with the VPE significantly suppressed, NWs doped primarily by the VLS mechanism have non-uniform dopant distribution along their axial direction. Figure 1.4 shows the doping profile in the axial direction of vertical GaAs NWs doped by diethyl-zinc

(DEZn) [36]. Although the GaAs NWs were doped primarily by the VLS mechanism, the carrier concentration increases along the growth direction towards the growth front.

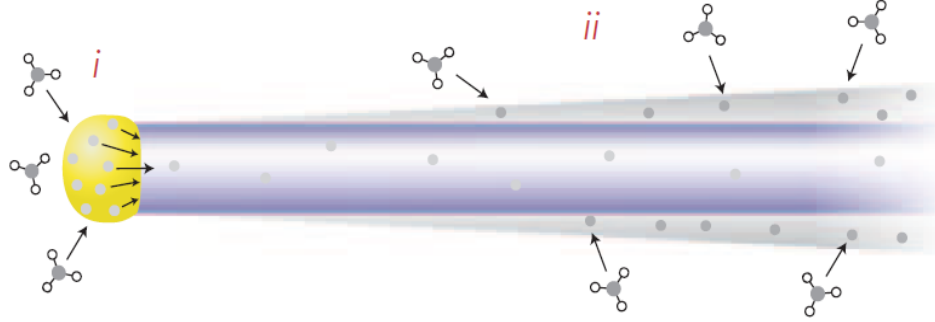


Figure 1.3: Illustration of two dopant incorporation paths in VLS NWs. The first path (i) is through the VLS growth mechanism: dopants dissolve in the alloy droplets and diffuse across the liquid-solid interface to the NW core. The second path (ii) is via the vapor phase epitaxy in which the dopants directly incorporate into the VPE shell around the NW. Reproduced from Reference [35].

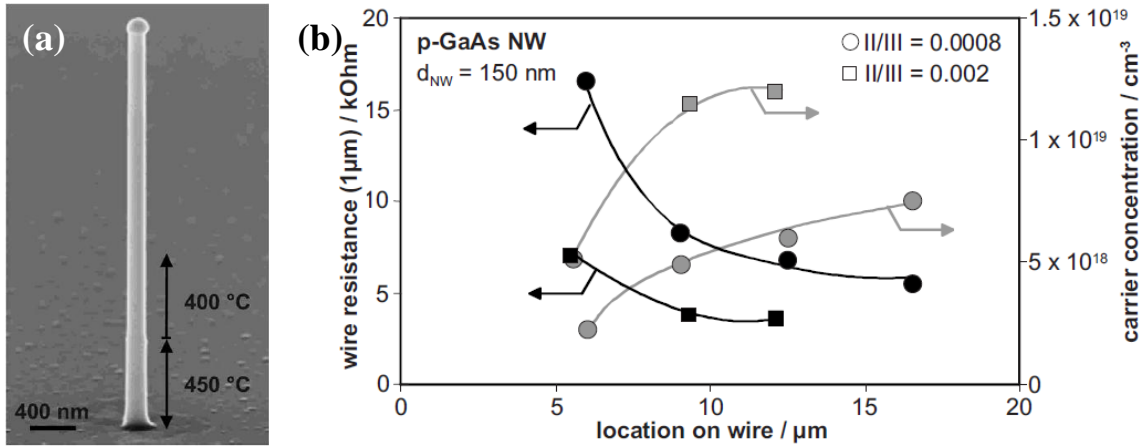


Figure 1.4: Zn doping profile along vertical GaAs NWs' axial direction. (a) Zn-doped vertical GaAs NW on a (111)B GaAs substrate grown at 400 °C with the initial growth at 450 °C. The VPE growth was effectively suppressed by the low growth temperature. (b) Carrier concentration and NW resistance along NWs' axial direction for two NWs doped with II/III ratios of 0.0008 and 0.002, respectively. Length zero represents the NW bottom. Reproduced from Reference [36].

Electrical techniques have been used to study the doping of VLS III-V NWs. The transmission line method (TLM) can measure the resistivity of doped NWs. Knowing the resistivity of NWs, the doping levels can be determined through data-fit process using transport models that include the effects from the doping level, carrier mobility and surface depletion [36]. NW FET transport models including the surface and body conduction can determine the doping levels of both the NW shells and cores [37]. By using a NW FET capacitance-voltage model to study the NW array-based capacitors, the conduction contribution from the shells and cores of NWs can also be separated [38].

Since electrical measurement senses the accumulative behavior of carriers from a large portion of a NW, high-resolution dopant distribution can hardly be achieved. Non-electrical dopant probing techniques have been used to scan along and across VLS III-V NWs for better spatial resolution. The atomic percentage of dopants in semiconductor materials can be measured through the energy dispersive X-ray spectroscopy (EDX), from which the doping level can be estimated [39]. Nanoscale free-carrier mapping was achieved by modeling the amplitude and phase of backscattered infrared light from an atomic force microscopy (AFM) tip placed in the proximity of the NWs [40]. The position and intensity of the local vibrational modes in Raman spectroscopy can give not only the spatial distribution but also the dope type of the dopants [41, 42]. Recently, three-dimensional (3D) high-resolution mapping of dopants in GaN [43] and GaAs [44] NWs were realized by using a so-called pulsed-laser atom probe tomography (APT) that had proved its success in characterizing the P distributions in VLS Ge NWs [35].

In order to have good doping control, careful selection of dopants and metal seeds is also important. Group II elements, such as Zn [36, 45] and Be [42, 46, 47], have been widely used as P-type dopants in III-V NWs. Group VI elements, such as Se [38] and Te [46], have been

reported as effective N-type dopants in III-V NWs. Group IV elements, such as C [48, 49] and Si [37, 41, 42], due to their amphoteric nature, can serve as either N-type or P-type dopants in III-V NWs. However, Sn, as a group IV element, was proved to be a good N-type dopant for InP [45], InAs [38] and GaAs [50]. Due to the different incorporation rate of dopants via the VPE and VLS growth mechanisms, dopants also have different incorporation rate into NWs' shells and cores. Be was reported to preferentially incorporate in the shells of GaAs NWs [47]; while Si was reported to selectively dope the cores of InAs NWs [37]. Excessive Zn and Be incorporation in III-V NWs can induce NW morphology changes, which places an upper bound on the achievable doping levels using these two types of dopants [36, 42, 51, 52]. Because of the dopants' different solid solubility and diffusion coefficient in the alloy droplets, using different metal seeds in the VLS growth can change the doping levels [53].

CHAPTER 2 – PLANAR NW HEMT

Semiconductor NW FETs are of great interest for future low-power and high-speed integrated circuits (ICs) because NWs' 3D feature enables a multi-gate device architecture for better control of the short channel effects (SCEs) [54, 55]. Bottom-up NWs do not require the expensive lithography and defective chemical etching to define and can serve as high-quality NW FETs channels. NW MESFETs [27, 56, 57], MISFETs [58-60] and HEMTs [61, 62] with VLS NW channels have all been demonstrated. However, bottom-up NW-based large-scale circuits are still a relatively unexplored area. The main challenges are controlled positioning of NWs, electrical uniformity, and compatibility with planar processing. To overcome these challenges, we demonstrate bottom-up grown planar-process compatible planar NW HEMTs with uniform and scalable DC characteristics [63].

2.1 Growth of planar NW HEMT

Unlike NW-FETs with vertical NW channels or post-growth externally aligned NW channels, planar NW FETs are very compatible with planar processing. The self-aligned growth feature also enables precise positioning of planar NWs via seed patterning techniques. Using VLS grown GaAs NWs as the channels [25], planar NW MESFETs have been demonstrated [27, 57]. Due to the uncertainty of the dopant distribution in VLS NWs [35, 47, 64], the electrical uniformity of the NW FETs with doped NW channels remains an issue.

We have proposed a planar NW HEMT structure with a core-shell NW heterostructure channel [65, 66] to resolve the electrical non-uniformity issue. The core-shell heterostructure channel is composed of undoped planar GaAs NWs (core) coated by a shared AlGaAs film

(shell). Figure 2.1a is the illustration of a planar GaAs NW HEMT with a single NW channel. Electrons (2DEG) at the interface between the AlGaAs shell and the GaAs NW core are remotely supplied from the doped AlGaAs film and modulated by the metal-AlGaAs Schottky gate (Figure 2.1b). Other than the recessed gate region, an n+ GaAs film is kept on top of the AlGaAs shell for making ohmic contacts. Because there is no intentional doping in the planar GaAs NW, the electrical properties of the NW HEMT are determined by the thickness and doping level of the AlGaAs shell. The shell growth on planar NWs is essentially the well-controllable thin film growth [67]. Thus, given planar NWs have uniform sizes, planar NW HEMTs with uniform electrical properties should be achieved.

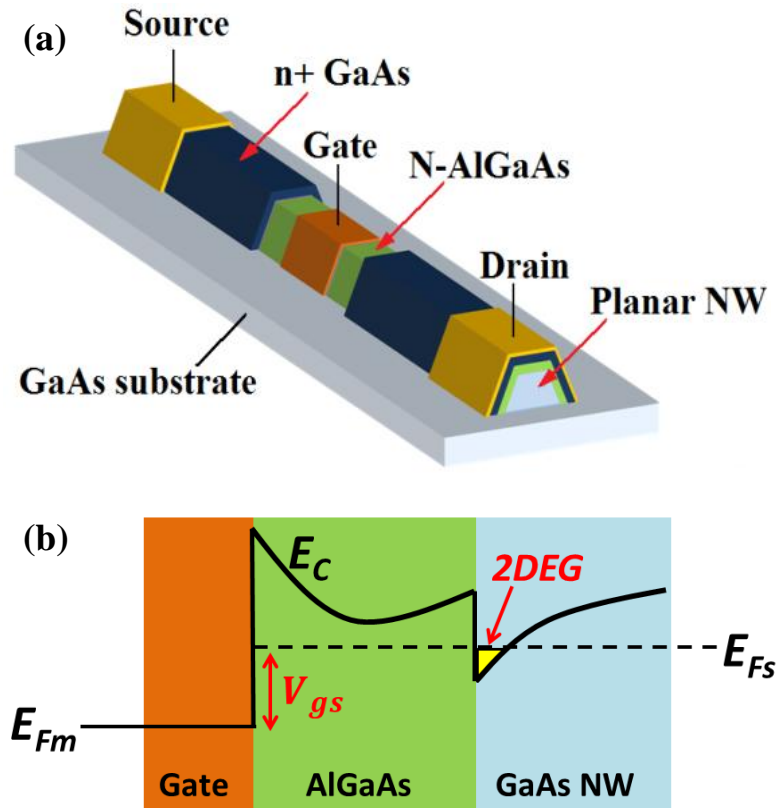


Figure 2.1: (a) Illustration of a planar GaAs NW HEMT with a single NW channel. The core-shell heterostructure channel is composed of an undoped planar GaAs NW (core) coated by an AlGaAs film (shell). The n+ GaAs film on top of the AlGaAs shell is the ohmic contact layer. (b) Band-diagram of the recessed gate region when device is conductive.

An Aixtron 200 MOCVD reactor was used for the growth of the planar NW HEMT sample. The precursors for Ga, Al, As and Si were trimethyl-gallium (TMGa), trimethyl-aluminum (TMAI), AsH₃ and Si₂H₆, respectively. Au colloids (metal seeds) with a uniform diameter of 250 nm were randomly dispersed on (100) semi-insulating (SI) GaAs substrates prior to the growth. Planar GaAs NWs along <110> directions were first grown via the Au-seeded VLS mechanism under atmospheric pressure at 460 °C with 5-sccm (5.78E-5 mol/min) TMGa flow and a nominal molar V/III ratio of 32. After the NW growth, the reactor pressure was lowered to 100 mbar, and the reactor temperature was raised to 680°C to for the following shell growth. A high shell growth temperature not only improves the quality of the shell films [68] but also suppresses the VLS NW growth [69, 70]. For the prototype devices, a 3-nm undoped Al_{0.35}Ga_{0.65}As spacer, 42-nm Si-doped ($2 \times 10^{18} \text{ cm}^{-3}$) Al_{0.35}Ga_{0.65}As barrier and 5-nm Si-doped GaAs ($5 \times 10^{18} \text{ cm}^{-3}$) ohmic contact layer were successively deposited on the planar GaAs NWs.

An as-grown planar NW HEMT heterostructure is shown in Figure 2.2. The sample was cleaved normal to the NW's axial direction. Citric acid: H₂O₂ (4:1) was used to selectively etch GaAs and reveal the details of the heterostructure. The dark void with a trapezoidal shape illustrates the planar GaAs NW which has two {111} sidewall facets and a (100) top facet (inset Figure 2.2). The bright film is the top Al_{0.35}Ga_{0.65}As barrier which is conformal to the planar GaAs NW. The Au seed locates at the far end of the NW.

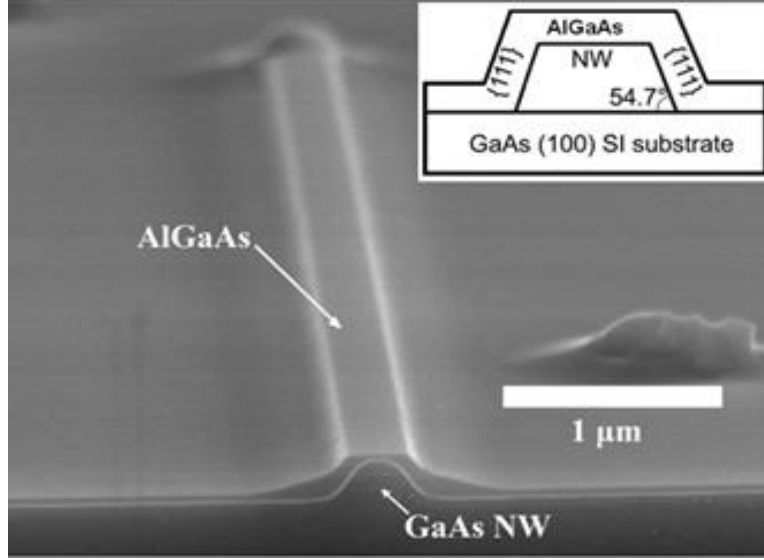


Figure 2.2: Cross-section scanning-electron-microscope (SEM) image of the NW HEMT heterostructure. Citric acid: H_2O_2 (4:1) was used to selectively etch GaAs and reveal the details of the NW heterostructure. The planar GaAs NW was seeded by an Au colloid with a diameter of 250 nm; and has a trapezoidal cross-section with a 140-nm (100) top facet and two 155-nm {111} sidewall facets (inset). The bright film is composed of a 3-nm $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}$ spacer and a 42-nm $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}$ top barrier. The Au seed is at the far end of the NW. Reproduced from Reference [63].

2.2 Fabrication and DC characteristics of planar NW HEMT

Since the planar NW HEMT structure is fully compatible with the planar processing, long-channel planar NW HEMTs were fabricated using the conventional optical lithography, wet etching and metallization processes. Source/drain ohmic contacts were done by annealing an electron-beam-evaporated metal stack of Ge/Au/Ni/Au (200/500/300/500 Å) in an H_2 environment at 400°C for 15 seconds. Because a thin GaAs ohmic contact layer was used, there was trivial leakage current among devices on the same chip. Therefore, the wet-etching mesa isolation step was skipped. Following the gate patterning, the gate recess etch was done using citric acid: H_2O_2 (4:1) to selectively remove the GaAs ohmic contact layer over the $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}$ barrier. After a brief HCl: DI (1:1) cleaning, the Ti/Au (100/1400 Å) gate metal stack was evaporated, which finalized the fabrication. Shown in Figure 2.3 are three planar GaAs

NW HEMTs that consist of single, double and triple NWs in the channels, respectively. The three devices have the same gate length (L_g) of $1.2\ \mu\text{m}$ and source-to-drain separation (L_{s-d}) of $5\ \mu\text{m}$. The planar GaAs NWs are with the same dimensions (see Figure 2.2) and perfectly parallel to each other due to the self-aligned growth feature.

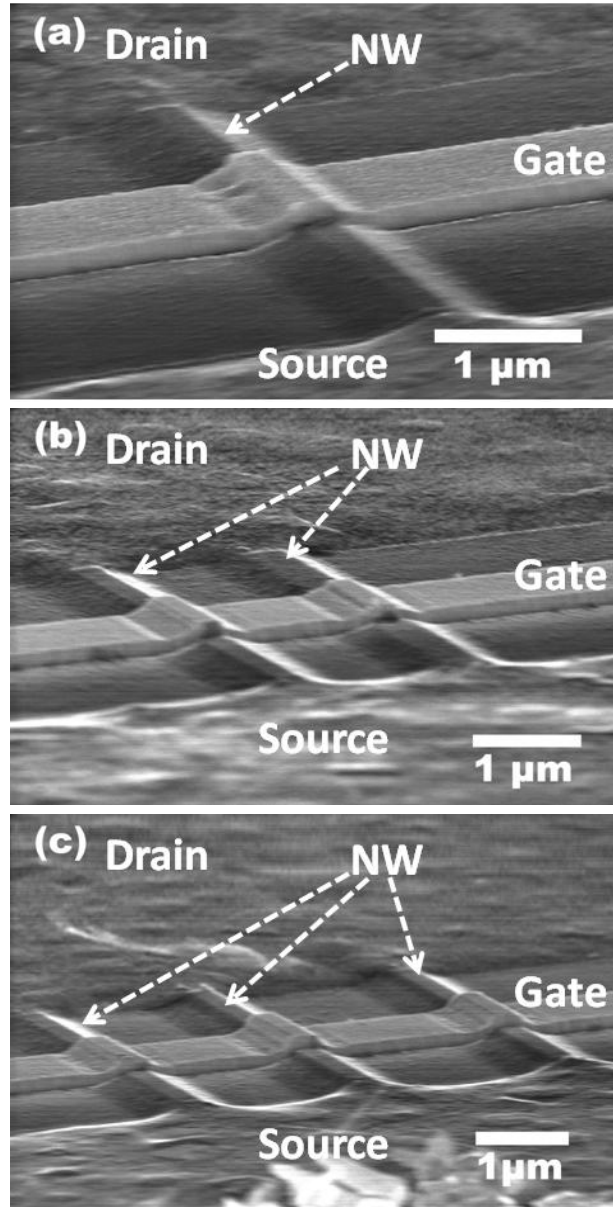


Figure 2.3: Tilt-view SEM images of three fully-processed planar GaAs NW HEMTs that consist of (a) single, (b) double and (c) triple NWs in the channels, respectively. The three devices have the same L_g of $1.2\ \mu\text{m}$ and L_{s-d} of $5\ \mu\text{m}$. Reproduced from Reference [63].

The DC characterization of the NW HEMTs was carried out on an Agilent 4155B semiconductor parameter analyzer (SPA). Source-to-drain I-V characteristics were measured for two-terminal single, double and triple NW devices similar to those shown in Figure 2.3 but without gate electrodes (Figure 2.4a). The current scales exactly with the number of NWs in the channels and increases linearly with the biasing voltage before reaching saturation. The I-V curve of a control device with no NWs in the channel is also shown in Figure 2.4a, which validates the low leakage among different devices. Figure 2.4b shows the output characteristics of the single, double and triple NW channeled planar NW HEMTs for V_{gs} from -1.5 V to 0.5 V in steps of 0.5V. The scaling of output current with the number of NWs in the channel is evident from the comparison of current levels of the three devices at the same V_{gs} . Figure 2.4c plots the transfer characteristics of all three devices for V_{ds} from 1.5 to 2.5 V in steps of 0.5 V. The inset of Figure 2.4c is the semi-log plots of the same transfer characteristics indicating that all devices have I_{on}/I_{off} of $\sim 10^4$. From Figure 2.4c and using the effective width per NW of 450 nm (see Figure 2.2), drive currents (I_{d-max}) of 100, 102 and 102 mA/mm at $V_{gs}=1$ V, peak extrinsic transconductances (G_{m-ext}) of 83, 84, and 86 mS/mm at $V_{ds}=2.5$ V, and subthreshold slope (SS) of 181, 173 and 160 mV/dec were extracted for the single, double and triple NW channeled planar NW HEMTs, respectively.

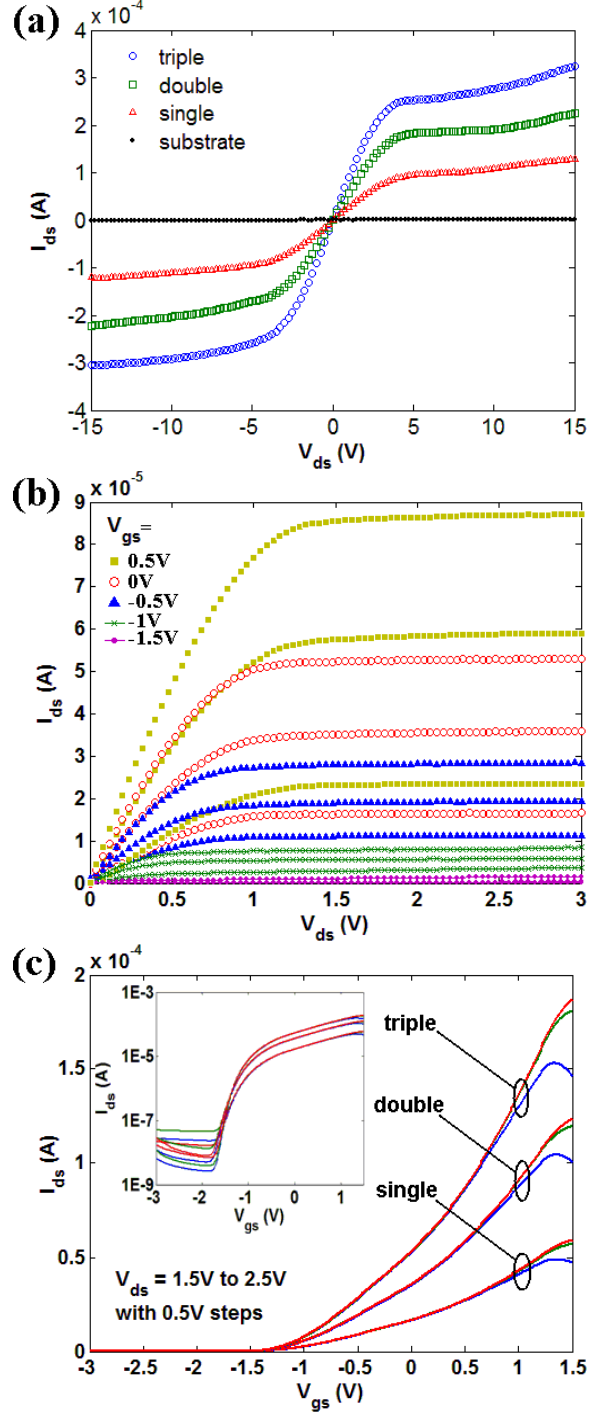


Figure 2.4: DC characteristics of single, double and triple NW channeled planar NW HEMTs as shown in Figure 2.3. (a) I-V characteristics of two-terminal single, double and triple NW devices similar to those shown in Figure 2.3 but without gate electrodes. (b) Output characteristics for V_{gs} from -1.5 V to 0.5 V in steps of 0.5V. Each set of color coded curves represent data taken from NW HEMTs with single (bottom), double (middle) and triple (top) NWs in the channel at the indicated V_{gs} . (c) $I_{ds} - V_{gs}$ transfer characteristics for V_{ds} from 1.5 to 2.5 V in steps of 0.5 V. Inset is the same $I_{ds} - V_{gs}$ curves in semi-log scale. Reproduced from Reference [63].

To evaluate the peak intrinsic transconductances (G_{m-int}), source-to-drain resistance of $16.24 \Omega \cdot \text{mm}$ was first extracted from the linear I-V of the single NW two-terminal device (the red coded curve in Figure 2.4a). Since the gate electrode of the fully-completed NW HEMT is in the middle of the source-to-drain region, half of the source-to-drain resistance can be assigned to the source access resistance (R_s). With the extracted R_s ($8.12 \Omega \cdot \text{mm}$), G_{m-int} of 255, 265 and 286 mS/mm at $V_{ds}=2.5 \text{ V}$ were estimated by $G_{m-ext}/(1 - R_s \cdot G_{m-ext})$ for the single, double and triple NW channeled planar NW HEMTs, respectively. The DC performance metrics of the single, double and triple NW channeled planar NW HEMTs are summarized in Table 2.1, confirming the uniform and scalable DC characteristics of the planar NW HEMTs.

Table 2.1: DC characteristics of planar NW HEMTs with single, double and triple planar NWs in the channels. Reproduced from Reference [63].

# of NWs in the channel	Single	Double	Triple
I_{d-max} (mA/mm) (at $V_{gs} = 1 \text{ V}$)	100	102	102
peak G_{m-ext} (mS/mm) (at $V_{ds} = 2.5 \text{ V}$)	83	84	86
peak G_{m-int} (mS/mm) (at $V_{ds} = 2.5 \text{ V}$)	255	265	286
V_T (V)	-1.5	-1.5	-1.5
SS (mV/dec)	181	173	119
I_{on}/I_{off}	10^4	10^4	10^4

For conventional film based HEMTs, the threshold voltage (V_T) can be estimated by

$$V_T \approx \phi_b - \frac{qN_d d_i^2}{2\epsilon_i} - \Delta E_c / q, \quad (2.1)$$

where Φ_b is the Schottky barrier height, q is the elementary electron charge, N_d , d_i and ϵ_i are the doping level, thickness and dielectric permittivity of the doped $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}$ top barrier, and ΔE_c is the conduction band offset between $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}$ and GaAs [71]. Based on the parameters used in the NW HEMTs ($\Phi_b = 1$ V, $N_d = 2 \times 10^{18} \text{ cm}^{-3}$, $d_i = 42$ nm, $\epsilon_i = 1.159 \times 10^{-12}$ F/cm, and $\Delta E_c = 0.244$ eV), we calculated a threshold voltage of -1.5 V which matches well to the experiment.

CHAPTER 3 – DOWN-SCALING OF PLANAR GAAS NW

In order to down-scale the NW based FETs, it is imperative to down-scale the sizes of NWs because enhanced 3D electrostatic gate control is only effective when the width of NW channels is smaller than the L_g of NW FETs. Since the diameter of VLS grown NWs depends on the size of Au seeds, Au seeds with small size should be used for growing down-scaled planar NWs. However, due to more severe parasitic sidewall film overgrowth, growth conditions need to be optimized for growing high-quality down-scaled planar NWs. Through mapping the growth parameters of TMGa flow, V/III ratio and temperature, we achieved high-quality sub-50-nm planar GaAs NWs [72].

3.1 Effect of group III flow

Planar GaAs NWs used in the prototype planar NW HEMTs (reported in Chapter 2) were grown under atmospheric pressure at 460 °C with 5 sccm (5.78×10^{-5} mol/min) TMGa flow, and a nominal molar V/III ratio of 32. Under the same growth conditions, planar GaAs NWs were grown using Au colloids with diameters of 250 nm, 100 nm and 20 nm on (100) GaAs SI substrates. Figure 3.1 shows the top-view and cross-section-view SEM images of the as-grown planar NWs for comparison. As can be seen, planar NWs seeded by 250-nm Au colloids have good morphology and smooth surfaces, while NWs seeded by 100-nm and 20-nm Au colloids have rough surfaces, more tapering along the axial direction, and notches perpendicular to the axial direction. The notches are correlated with twin defects from TEM inspection [52], which has also been reported in studies on III-V vertical NWs [8, 73, 74]. Rough surfaces, tapering and

twin-plane defects are detrimental for the carrier mobility and electrical uniformity of the planar NW and need to be eliminated.

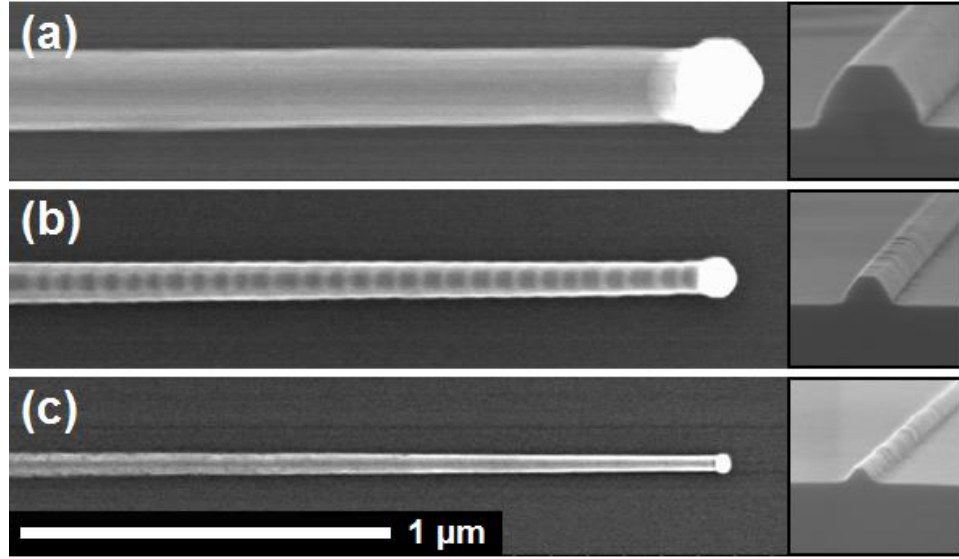


Figure 3.1: Top-view and cross-section-view SEM images of the as-grown planar NWs seeded by Au colloids with (a) 250-nm, (b) 100-nm and (c) 20-nm diameters on (100) SI GaAs substrates under atmospheric pressure at 460 °C with 5 sccm ($5.78\text{E-}5$ mol/min) TMGa flow, and a nominal molar V/III ratio of 32. All images share the same scale bar. Reproduced from Reference [72].

The effect of TMGa flow on planar NW growth was studied by growing 100-nm and 20-nm Au colloid-seeded planar NWs under the same conditions as mentioned above except with various TMGa flows from 2.5 sccm to 10 sccm. The growth time (t_g) was 140 seconds for all growth experiments. Each sample was inspected in SEM after the growth; and the averages of the NW length (L_{NW}), bottom cross-section width at the beginning (W_b) and end (W_e) of planar NWs were extracted. The axial growth rate (R_{axial}) of the planar NW is $\frac{L_{NW}}{t_g}$. The radial growth rate (R_{radial}) of the parasitic film is $\frac{(W_b - W_e) \times \sin(54.7^\circ)}{2 \times t_g}$, considering the isosceles-trapezoidal (with base angle of 54.7°) shape of planar NWs. The tapering factor, namely R_{radial}/R_{axial} ,

denotes the thickness of parasitic film deposited in the radial direction per μm increment of NW in the axial direction. Figure 3.2 plots the R_{axial} and R_{radial} of 100-nm and 20-nm Au colloid-seeded planar NWs with various TMGa flows. As the TMGa flow increases, R_{axial} increases significantly while R_{radial} stays relatively the same, which helps to reduce the tapering factor from 7.9 nm/ μm to 2.4 nm/ μm and 8.4 nm/ μm to 1.5 nm/ μm for 100-nm and 20-nm Au colloid-seeded NWs, respectively. The stronger correlation between R_{axial} and the TMGa flow is a clear evidence of the catalytic effect of Au colloids which selectively enhance the pyrolysis of TMGa on site. From the experimental results, large group III flow would lead to less tapered planar NWs.

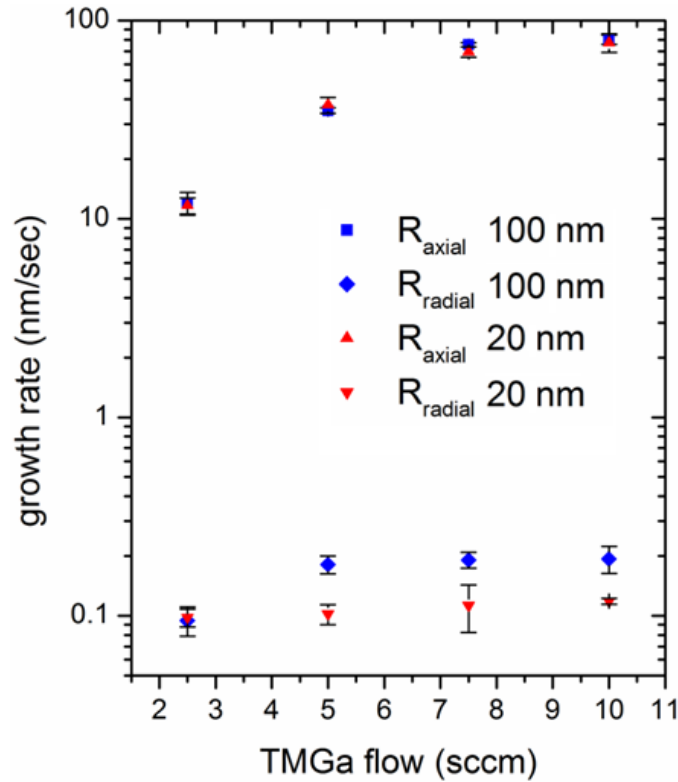


Figure 3.2: R_{axial} (upper marks) and R_{radial} (lower marks) of 100-nm (blue squares) and 20-nm (red triangles) Au colloid-seeded planar GaAs NWs under atmospheric pressure at 460 °C with a nominal molar V/III ratio of 32 but various TMGa flows. Reproduced from Reference [72].

3.2 Effect of V/III ratio

The effect of V/III ratio on planar NW growth was then investigated by growing 100-nm and 20-nm Au colloid-seeded planar NWs under atmospheric pressure at 460 °C with 10-sccm TMGa flow but various V/III ratios of 32, 16, 8 and 4. The R_{axial} , R_{radial} and tapering factor were obtained for NWs grown for 140 seconds. Figure 3.3 plots the R_{axial} and R_{radial} of 100-nm and 20-nm Au colloid-seeded planar NWs with various V/III ratios. As the V/III ratio decreases, R_{axial} increases slightly while R_{radial} decreases, which further reduces the tapering factor from 2.4 nm/ μm to 1.1 nm/ μm and 1.5 nm/ μm to 0.8 nm/ μm for 100-nm and 20-nm Au colloid-seeded NWs, respectively. As reported for III-V vertical NWs, both R_{axial} and R_{radial} decrease with the decrease of the V/III ratio [75]. The different dependence of R_{axial} on V/III ratio for III-V planar and vertical NWs may be attributed to the easier diffusion access of growth species to planar-NW seeds than vertical-NW seeds. From Figure 3.3, in the range of study, low V/III ratio renders less tapered planar NWs.

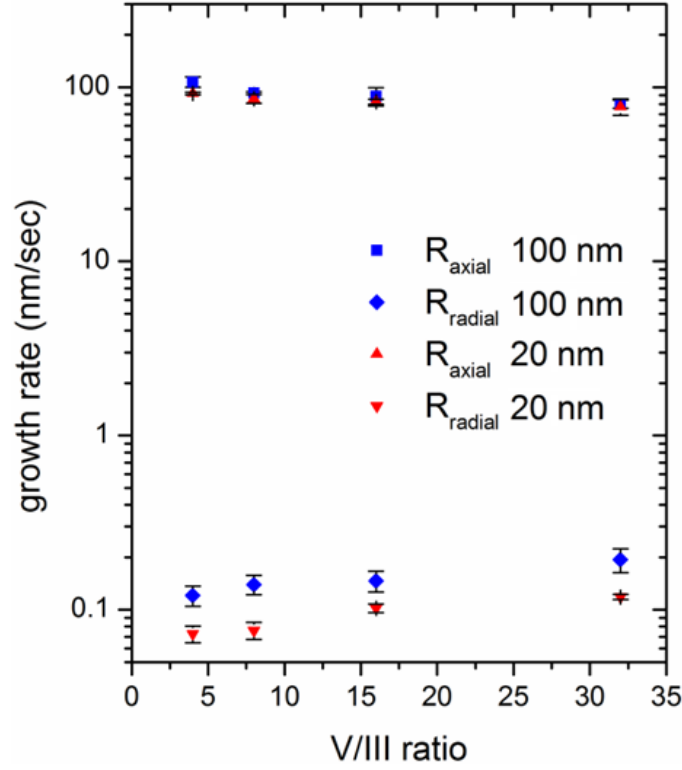


Figure 3.3: R_{axial} (upper marks) and R_{radial} (lower marks) of 100-nm (blue squares) and 20-nm (red triangles) Au colloid-seeded planar GaAs NWs under atmospheric pressure at 460 °C with 10-sccm TMGa flow but various V/III ratios. Reproduced from Reference [72].

3.3 Effect of growth temperature

With the optimization of TMGa flow and V/III ratio, twin defects induced notches still exist in planar GaAs NWs seeded by Au colloids with diameters less than 150 nm and grown under atmospheric pressure at 460 °C. Low growth temperature has been proven to reduce the twin-defect density and promote pure ZB phase for VLS vertical III-V NWs [9]. Therefore, growth temperature modulation was implemented to grow twin-defect-free down-scaled planar NWs.

As has been reported [25], the yield of planar NW is growth temperature related. If GaAs NWs are grown at temperature well below 460 °C, NWs prefer to grow out of plane along the $\langle 111 \rangle_B$ directions rather than in plane along the $\langle 110 \rangle$ directions, which reduces the yield of

planar NW. In order to grow planar NWs at low temperature but maintain high yield, we adopted a so-called two-temperature-step growth method [76] as illustrated in Figure 3.4. As can be seen, the growth temperature is first kept at 460 °C for 20 seconds, then ramped down to and maintained at a target temperature (T_{target}). The planar NW growth is initiated at 460 °C. During the following low temperature growth, planar NWs tend to keep growing in-plane with the substrate. Thus, the yield of planar NWs in such two-temperature-step growth is the same as in constant 460-°C growth. However, there is still a lower bound of the T_{target} : when the T_{target} is below 425 °C, planar GaAs NWs would take off and grow along the $\langle 111 \rangle_B$ directions.

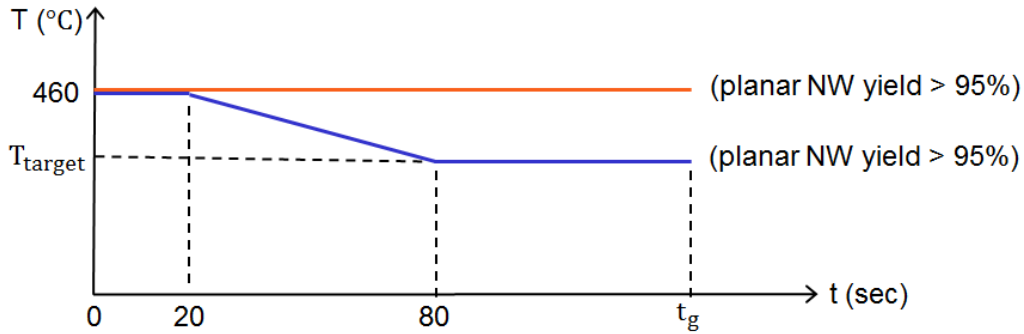


Figure 3.4: Illustration of the two-temperature-step growth method (blue) which keeps the planar NW yield unchanged in comparison with the constant temperature growth at 460 °C (orange).

In a group of controlled growth experiments, GaAs NWs were grown with the T_{target} , t_g and TMGa flow set to 435 °C, 140 seconds and 10 sccm respectively, but the V/III ratio was adjusted. When a V/III ratio of 6 was used, as shown in Figure 3.5a, 250-nm and 150-nm Au colloid-seeded planar GaAs NWs have smooth sidewall facets while the 100-nm Au colloid-seeded planar GaAs NWs have twin defects induced notches. With a change of the V/III ratio from 6 to 4, planar GaAs NWs seeded by Au colloids with diameters above 20 nm (the smallest used in the experiments) are completely notch-free. Figure 3.5b shows a notch-free sub-50-nm planar GaAs

NW seeded by a 20-nm Au colloid with a V/III ratio of 4. Thus, an appropriate combination of low growth temperature and a V/III ratio is the key to eliminate the twin defects induced notches in planar NWs; and the smaller the planar NW is, the lower the V/III ratio needs to be.

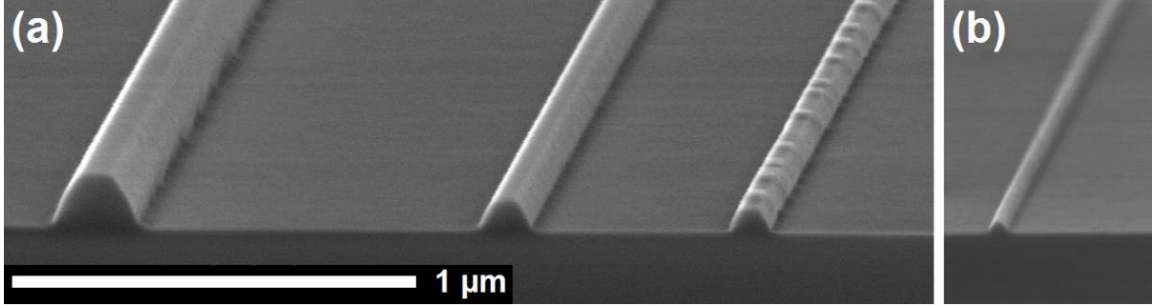


Figure 3.5: (a) Cross-section-view SEM image of three planar GaAs NWs seeded by 250-nm, 150-nm and 100-nm Au colloids (from left to right) under V/III ratio of 6 using a two-temperature-step (460 → 435 °C) growth method. The notches in 100-nm Au colloid-seeded planar NW were induced by twin defects. (b) Notch-free sub-50-nm planar GaAs NW seeded by a 20-nm Au colloid with the change of V/III ratio from 6 to 4. All images share the same scale bar. Reproduced from Reference [72].

The R_{axial} , R_{radial} and tapering factor were extracted for the planar GaAs NWs grown using the two-temperature-step growth method. The R_{radial} in the two-temperature-step growth is lower than that in the constant 460-°C growth due to the lower pyrolysis rate of the growth species at low temperature. However, the R_{axial} in the two-temperature-step growth is higher than that in the constant 460-°C growth because of the minor temperature effect on the Au-catalyzed pyrolysis rate of the growth species and the effectively increased growth supply from the decreased radial growth. As a result, the two-temperature-step growth method also improves the tapering factor of planar NWs. The detailed two-temperature-step growth parameters of 100-nm Au colloid-seeded planar GaAs NWs are summarized in Table 3.1 for reference.

Table 3.1: Two-temperature-step growth parameters of 100-nm Au colloid-seeded planar GaAs NWs.

diameter of Au colloid (nm)	100
MOCVD reactor pressure (mbar)	950
growth time (sec)	140
growth temperature (°C)	460 → 435
TMGa molar flow rate (mol/min)	1.16E-4
AsH ₃ molar flow rate (mol/min)	4.46E-4
average R _{axial} (nm/sec)	179
average R _{radial} (nm/sec)	0.08
tapering factor (nm/μm)	0.45

In summary, we have successfully grown notch-free high-quality sub-50-nm planar GaAs NWs by using a two-temperature-step (460 → 435°C) growth method with optimized TMGa flow of 10 sccm and V/III ratio of 4.

CHAPTER 4 – BARRIER-ALL-AROUND PLANAR NW HEMT

Monolithic barrier-all-around (BAA) planar NW HEMT was made through growth mode modulation for the AlGaAs back-barrier, planar GaAs NW channel and AlGaAs top barrier. Owing to the down-scaled 3D planar NW channel, a BAA planar NW HEMT with L_g of 120 nm has peak G_{m-ext} of 550 $\mu S/\mu m$ and I_{d-max} of 435 $\mu A/\mu m$. The excellent DC characteristics of the BAA planar NW HEMT demonstrates the potential of using the bottom-up planar NW technology for future low power and high speed very large scale circuits (VLSI) [72].

4.1 Growth of BAA planar NW HEMT

With the capability of growing down-scaled planar GaAs NWs, down-scaling of planar NW HEMTs is possible (as reasoned in Chapter 3). However, the thermal stability of the down-scaled planar GaAs NWs became a new problem. After the growth of the AlGaAs top barrier at the typical temperature of 680 °C, sub-100-nm planar GaAs NWs were found deformed into flat shapes. Shown in the top inset of Figure 4.1 is a deformed planar GaAs NW seeded by a 20-nm Au colloid with the top $Al_{0.33}Ga_{0.67}As$ barrier selectively etched. Clearly, deformed planar NWs have low aspect ratio and lose the advantage of 3D electrostatic control.

Growing the $Al_{0.33}Ga_{0.67}As$ top barrier at lower temperature of 600 °C still rendered deformed planar GaAs NWs. Since low growth temperature does not produce high-quality doped $Al_{0.33}Ga_{0.67}As$, growing the top barrier at temperature < 600 °C is unwanted. To solve the problem, we developed a two-temperature-step method of growing the top epitaxial layers: coat and protect the planar GaAs NWs with the 3-nm undoped $Al_{0.33}Ga_{0.67}As$ spacer grown at 500 °C, then deposit the doped top $Al_{0.33}Ga_{0.67}As$ barrier and GaAs ohmic contact layer at 680 °C.

Because undoped $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ is much less diffusive than GaAs, the low-temperature $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ spacer can stabilize the surface atoms of the GaAs NWs and maintain GaAs NWs' original morphology throughout the following high temperature processes. Figure 4.1 shows the preserved planar NW HEMT structures with 20-nm Au colloid-seeded NW channels using such two-temperature-step epitaxial growth method.

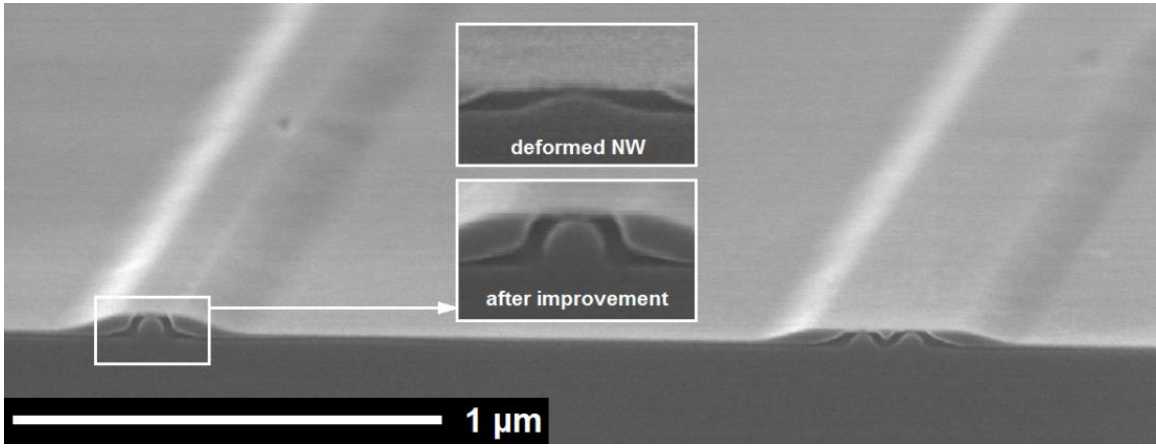


Figure 4.1: Cross-section-view SEM image of as-grown planar NW HEMT structures with 20-nm Au colloid-seeded NW channels using the two-temperature-step ($500 \rightarrow 680^\circ\text{C}$) epitaxial growth method. The $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ top barrier was selectively etched by diluted HF. The insets illustrate two NW HEMT structures with deformed (top) and preserved (bottom) planar GaAs NW channels (all NWs were seeded by 20-nm Au colloids). Reproduced from Reference [72].

In order to enhance the carrier confinement in the NW channel, a monolithic BAA planar NW heterostructure was used for device fabrication. A (100) SI GaAs substrate with dispersed 50-nm Au colloids was loaded in the MOCVD reactor for the growth. Prior to the VLS NW growth, an undoped 150-nm thick $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ back barrier was grown under low reactor pressure (100 mbar) and at 680°C , during which the Au colloids elevated to the top surface of the newly-grown $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ and no NW growth took place [25]. Then 15- μm long undoped planar GaAs NWs were grown under atmospheric reactor pressure using the two-temperature-

step ($460 \rightarrow 435$ °C) VLS growth method discussed in Chapter 3. With the reactor pressure adjusted to 100 mbar, a 3-nm undoped $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ spacer, a thick Si-doped ($2 \times 10^{18} \text{ cm}^{-3}$) $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ top barrier and an n^+ ($5 \times 10^{18} \text{ cm}^{-3}$) GaAs ohmic contact layer were successively deposited on the planar GaAs NWs using the two-temperature-step method ($500 \rightarrow 680$ °C) mentioned above. The cross-section of the as-grown BAA planar NW heterostructure is shown in Figure 4.2 where the $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ was selectively etched by diluted HF to reveal contrast. From Figure 4.2, the periphery of the NW's conducting surfaces (a top and two sidewall facets) is 145 nm, which is also the effective channel width per NW.

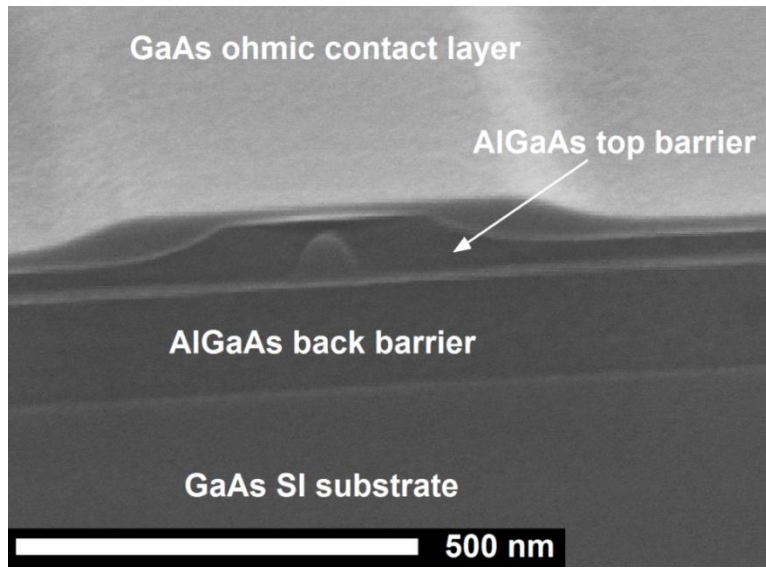


Figure 4.2: Cross-section-view SEM image of a representative BAA planar NW heterostructure. The $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ was selectively etched by dilute HF to reveal contrast. The periphery of the NW's conducting surfaces (a top and two sidewall facets) is 145 nm. Reproduced from Reference [72].

4.2 Fabrication and DC characteristics of BAA planar NW HEMT

After growth, source and drain with 3- μm separation were patterned through optical lithography. Ni/Ge/Au/Ni/Au (50/200/500/300/500 Å) ohmic metal stack was evaporated with

an electron-beam evaporator followed by liftoff and rapid thermal annealing. Mesa isolation (200 nm in depth) was formed by wet etch in $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{DI}$ (1:8:80) for 25 seconds. A 120-nm gate was patterned by electron-beam lithography (EBL). Gate recess etch was done in citric acid: H_2O_2 (4:1) for 5 seconds during which the GaAs ohmic contact layer was selectively removed. After 20-second etch-residue cleaning in $\text{HCl}:\text{DI}$ (1:1), Ti/Au (100/1400 Å) gate metal stack was evaporated followed by liftoff. A fully-fabricated BAA planar NW HEMT with a single GaAs NW channel as shown in Figure 4.2 is shown in Figure 4.3.

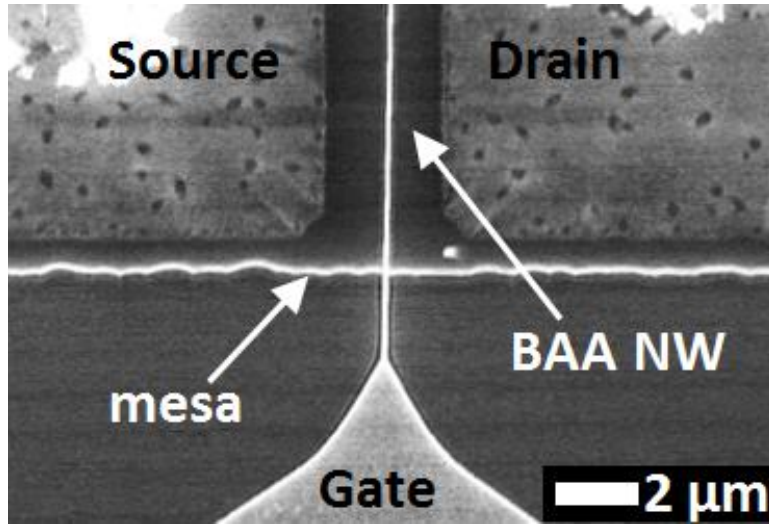


Figure 4.3: Top-view SEM image of a fully-fabricated short-channel BAA planar NW HEMT with a 120-nm gate, source-to-drain separation of 3 μm and a single GaAs NW channel as shown in Figure 4.2. Reproduced from Reference [72].

The DC measurement was done with a Keithley 4200 semiconductor characterization system (SCS). Figure 4.4a shows the output characteristics for V_{gs} from -0.9 V to 0.5 V in steps of 0.2 V. Figure 4.4b plots the transfer characteristics at $V_{\text{ds}} = 2$ V scaled by the effective channel width of 145 nm (Figure 4.2). The peak $G_{\text{m-ext}}$ is 550 $\mu\text{S}/\mu\text{m}$ and $I_{\text{d-max}}$ is 435 $\mu\text{A}/\mu\text{m}$. Figure 4.4c is the semi-log transfer characteristics for V_{ds} from 0.5 V to 2.5 V in steps of 0.5 V, from

which $I_{\text{on}}/I_{\text{off}}$ of 10^4 , SS of 160 mV/dec and drain-induced barrier lowering (DIBL) of 120 mV/V were extracted. Since the device reveals enhancement-mode operation, precise gate recess etch is essential for optimal performance. Under-etching would leave parasitic n+ GaAs channel on top of the $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ barrier which degrades the $I_{\text{on}}/I_{\text{off}}$, SS and DIBL. Over-etching would create two exposed $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}/\text{GaAs-NW}$ regions beside the metal gate, which increases the source/drain access resistance and reduces the $I_{\text{d-max}}$ and $G_{\text{m-ext}}$.

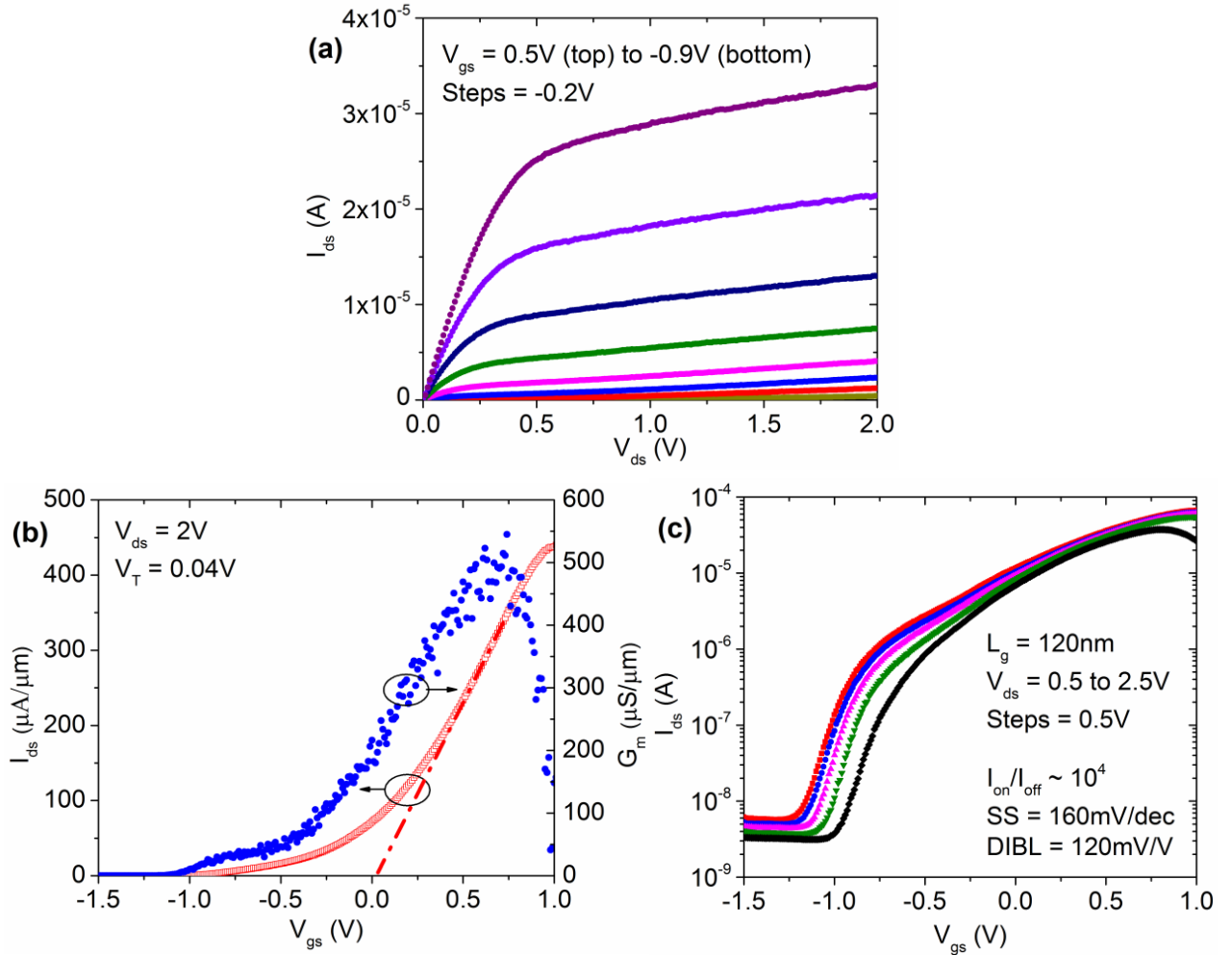


Figure 4.4: DC characteristics of the BAA planar NW HEMT as shown in Figure 4.3. (a) Output characteristics for V_{gs} from -0.9 V to 0.5 V in steps of 0.2 V. (b) Transfer characteristics at $V_{\text{ds}} = 2\text{ V}$ scaled by the effective channel width of 145 nm. (c) Semi-log transfer characteristics for V_{ds} from 0.5 V to 2.5 V in steps of 0.5 V. Reproduced from Reference [72].

The effective electron velocity (v_{eff}) was also extracted by using the relationship $G_{\text{m-int}}/C_{\text{ox}}$ [77], where $G_{\text{m-int}}$ is the intrinsic transconductance and C_{ox} is the gate capacitance per unit area. $G_{\text{m-int}}$ was calculated by $G_{\text{m-ext}}/(1 - R_s \cdot G_{\text{m-ext}})$, in which R_s (the source access resistance) was approximated as 25% of the transistor's on resistance considering the thick $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ top barrier. C_{ox} can be expressed as $\epsilon/(d + \Delta d)$, where ϵ is the gate dielectric permittivity, d is the effective distance from gate to channel interface and Δd is the distance from the channel interface to electrons' peak position. By averaging the total gate capacitance contributed from two incline-plate capacitors (gate to NW sidewall facets) and one parallel-plate capacitor (gate to NW top facet), d was estimated to be 38 nm. For the $\text{AlGaAs}/\text{GaAs}$ interface, $\Delta d=8$ nm was assumed [78]. The extracted v_{eff} for our BAA planar NW HEMT is $\sim 2.9 \times 10^7$ and $2.6 \times 10^7, 1.7 \times 10^7$ cm/s at $V_{\text{ds}} = 2, 1$, and 0.5 V respectively. Table 4.1 benchmarks the performance of our BAA planar NW HEMT against the state-of-art III-V FETs in other geometries, including InGaAs quantum well (QW) HEMTs [79], top-down etched planar InGaAs NW and VLS vertical InAs NW gate-all-around (GAA) MOSFETs [80, 81]. The same method was used for the v_{eff} extraction of other devices.

Table 4.1: Benchmarking of device performance. Reproduced from Reference [72].

Ref.	Geometry	L_g (nm)	V_{dd} (V)	$I_{\text{d-max}}$ (A/mm)	$G_{\text{m-ext}}$ (S/mm)	SS (mV/dec)	Estimated v_{eff}^* ($\times 10^7$ cm/s)
This work	GaAs NW-HEMT	120	1.0	0.38	0.50	160	2.6
[79]	$\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QW-HEMT	40	0.6	0.96	2.70	115	3.0
[80]	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ GAA-MOS	20	0.5	0.63	1.74	88	1.2
[81]	InAs GAA-MOS	100	0.5	0.60	1.23	140	0.6

*Parameters used for v_{eff} estimation of referenced devices are from the referenced work.

Although having the largest L_g , our BAA planar NW HEMT is among the best in v_{eff} , indicating excellent channel material property. Other DC performance metrics can be readily improved by adopting a delta-doped thin AlGaAs top barrier which not only enhances the gate's electrostatic control but also reduces the source/drain access resistance.

CHAPTER 5 – LARGE-SCALE PLANAR NW ARRAY

Planar NWs grown via dispersed Au colloids have two drawbacks: random positioning and broad NW-size distribution. In order to make the planar NW technology feasible for large-scale application, growth technique with precise NW site and size control need to be developed. Through process optimization, we demonstrated large-scale planar NW arrays grown from top-down lithography and liftoff defined Au seeds.

5.1 Growth of planar NW array from optical lithography defined seeds

An aperture-based contact optical lithography was used for low-cost sub-micron patterning of Au seeds [82]. The lithography ‘mask’ is a polydimethylsiloxane (PDMS) template that comprises arrays of metal-coated PDMS pyramids with an aperture at each pyramid tip. Before exposure, the template was brought in contact with photoresist-coated (100) SI GaAs substrates. Exposure was done through the pyramid apertures with H-Line (405 nm) UV light fed into the PDMS template. Typical tetramethylammonium hydroxide (TMAH) based developer was used for sample developing. Figure 5.1 is the top-view optical image of a developed sample. The PR openings have circular shape with diameters of ~600 nm. Before Au evaporation, the developed sample was put in oxygen plasma and in HCl:DI (1:1) for 30 and 15 seconds respectively for the removal of possible PR residues in the openings. Since the volume of the Au seed determines the size of the seeded NW, a thin layer of Au with thickness of 15 nm was deposited to grow small NWs.

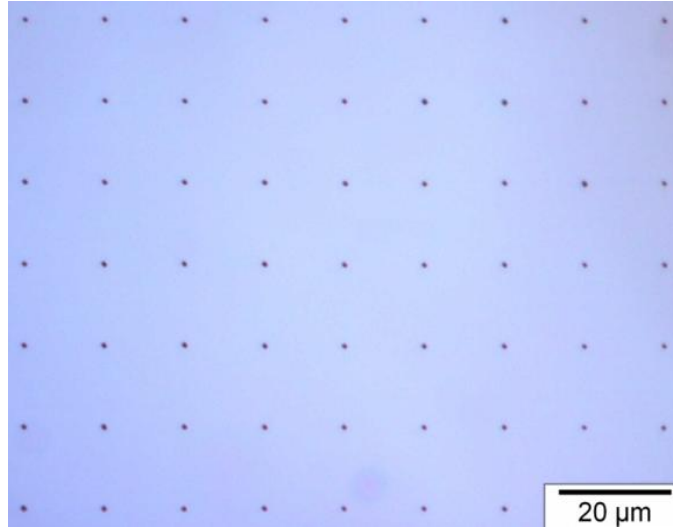


Figure 5.1: Top-view optical image of a developed sample patterned by the aperture-based contact optical lithography. The PR openings have circular shape with diameters of ~ 600 nm.

Because planar NWs have epitaxial relation with the substrate, stringent cleaning after Au liftoff is essential for high planar NW yield. Hot AZ 400T PR stripper and HCl:DI (1:1) were found very effective in removing the organic residues and were used in the cleaning process. The cleaned sample was finally loaded in an Aixtron 200 MOCVD reactor for GaAs NW growth under atmospheric pressure at 460°C with 5-sccm TMGa flow and V/III ratio of 32. Figure 5.2 shows the tilt-view SEM image of the as-grown sample. As can be seen, the planar NW yield is moderate. However, at some of the patterned sites, multiple NWs from one patterned Au seed can be observed. This is probably due to the splitting of the low-aspect-ratio Au seeds at the pre-growth annealing stage of the growth. A zoom-in image of an out-of-plane GaAs NW is also shown in Figure 5.2. A disk-like shallow mesa at the footprint of the NW can be seen. The formation of the mesa could be from the alloying of the low-aspect-ratio Au seed with the GaAs substrate during the pre-growth annealing. Clearly, the NW is planar on the mesa and is out of plane off the mesa. Therefore, patterned Au seeds with small diameters and high aspect ratios are

required for making planar NW arrays with high yield and one-to-one seed-to-NW correspondence.

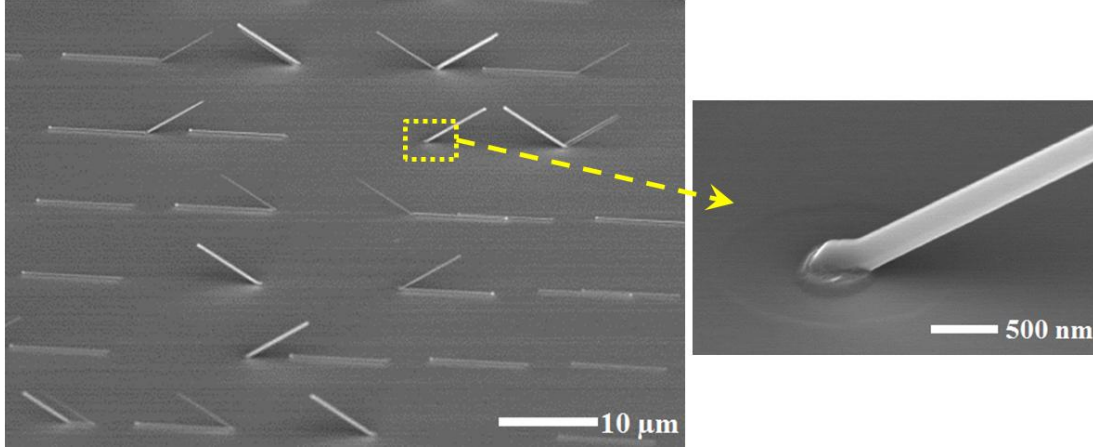


Figure 5.2: Tilt-view SEM image of GaAs NWs grown from Au seeds patterned by the aperture-based contact optical lithography. The inset is the zoom-in footprint of an out-of-plane NW.

5.2 Growth of planar NW array from electron-beam lithography defined seeds

In order to make Au seeds with small diameters and high aspect ratios, electron-beam lithography (EBL) was used for patterning. Arrays of Au seeds (disk-like) with diameters of 50 to 300 nm, the same height of 50 nm and center-to-center separations of 100 to 500 nm were patterned on (100) SI GaAs substrates by EBL, metal evaporation and liftoff processes. Hot Remover-PG resist stripper and HCl:DI (1:1) were used to clean the sample before the NW growth. The growth of planar GaAs NW arrays was carried out in an Aixtron 200 MOCVD reactor using the two-temperature-step ($450 \rightarrow 435^\circ\text{C}$) growth method detailed in Chapter 3 [72].

Figure 5.3 shows a tilt-view SEM image of a representative planar NW array with 100% yield and one-to-one seed-to-NW correspondence. The planar GaAs NWs grow bi-directionally in the anti-parallel $[0-11]$ and $[01-1]$ directions (left and right in Figure 5.3), with respective lengths of ~ 22 and $28 \mu\text{m}$ for 140-second growth. Because of the bi-directionality, the grown

NWs are no longer equally spaced; and whenever there are missing NWs in the array propagating to one side, they can surely be found on the other side. The insets, from the left to the right, are the patterned Au seeds (100-nm diameter, 300-nm separation and 50-nm height), the zoom-in images of the dividing line between the oppositely propagated NWs and the tips of the [01-1] planar NWs. The tiny out-of-plane GaAs whiskers at the dividing line are originated from tiny Au particle residues split from the patterned Au seed array. The cross-section of a cleaved planar NW array is shown in Figure 5.4. The planar NWs appear trapezoidal with perfectly uniform dimensions. With the patterned planar NW growth technique, large-scale planar NW arrays were achieved, indicating the potential of our planar-NW technology for wafer-scale device and circuit applications. Figure 5.5 shows the top-view of large-scale VLS grown planar GaAs arrays.

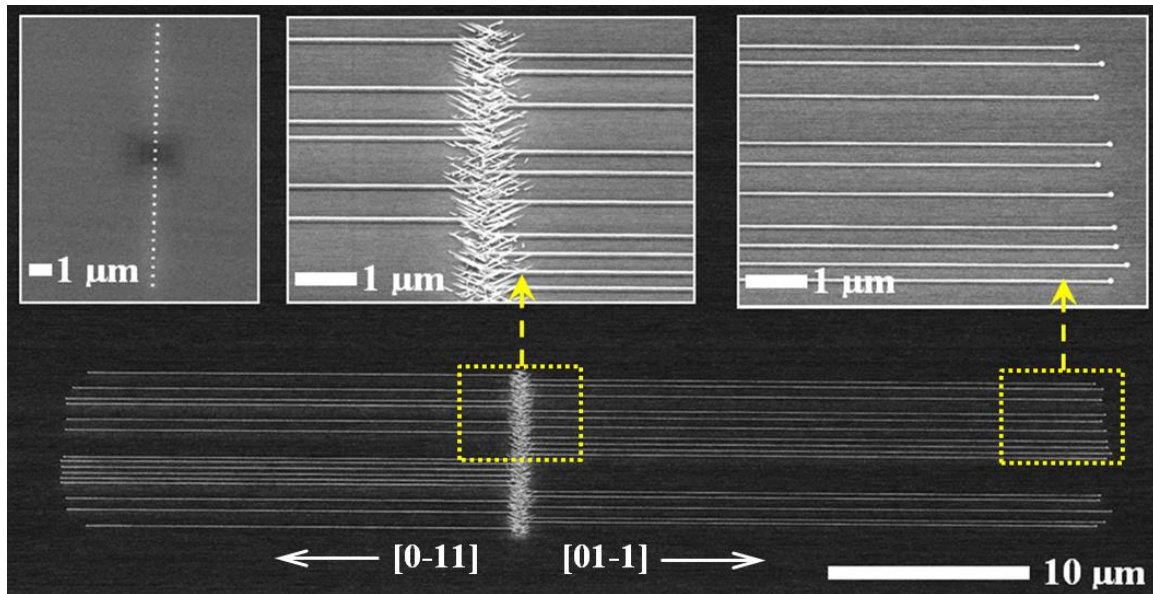


Figure 5.3: Tilt-view SEM image of a representative planar NW array with 100% yield and one-to-one seed-to-NW correspondence. The insets, from the left to the right, are the patterned Au seeds (100-nm diameter, 300-nm separation and 50-nm height), the zoom-in images of the dividing line between the oppositely propagated NWs and the tips of the [01-1] planar NWs.

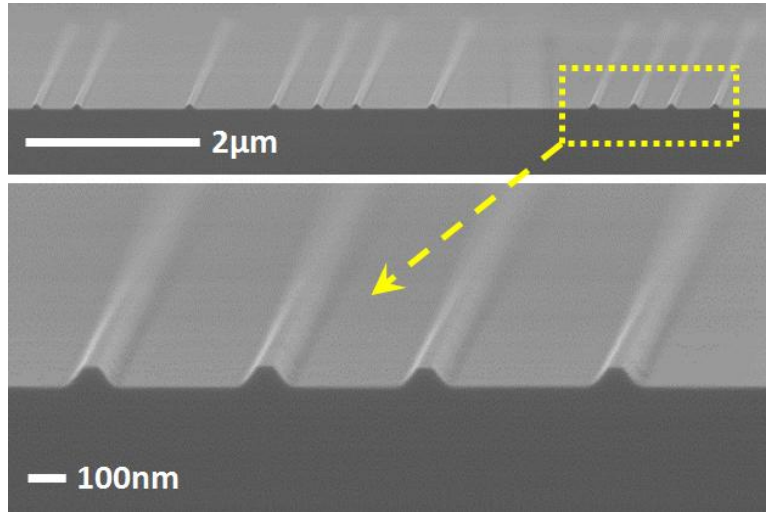


Figure 5.4: Cross-section-view SEM image of a cleaved planar NW array.

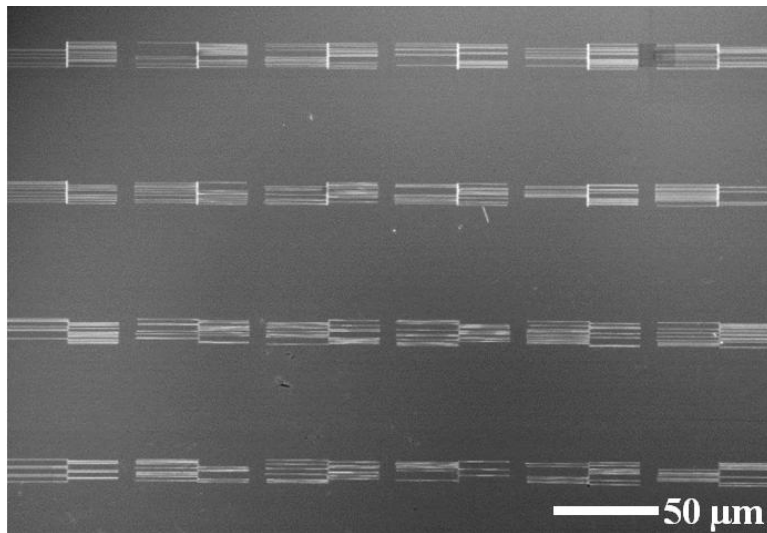


Figure 5.5: Top-view SEM image of large-scale VLS grown planar GaAs arrays.

CHAPTER 6 – WAFER-SCALE ARRAY-BASED PLANAR NW HEMT

For the first time, using the site-controlled planar NW growth method (detailed in Chapter 5), we demonstrated monolithically integrated planar NW array-based HEMTs with densely-packed planar NWs in the channel. The NW HEMTs operate in enhancement-mode and have excellent DC/RF performances with $I_{\text{on}}/I_{\text{off}} \sim 10^4$, $SS \sim 102$ mV/dec, $DIBL \sim 151$ mV/V and $f_T/f_{\text{max}} \sim 33/75$ GHz. With biasing less than 1 V, the f_T/f_{max} is $\sim 37/67$ GHz. The results place our bottom-up planar-NW transistor technology a strong candidate for future low-power and high-speed VLSI. To our knowledge, the f_{max} achieved here is higher than any nanoscale device with VLS NWs, CNTs, or 2D sheets aligned in-plane with the substrate.

6.1 Growth of planar NW array-based HEMT

Vertical III-V NWs are easily accessible through VLS growth on (111)B substrates [4]. Through seed patterning techniques [83], vertical III-V NW array-based transistors have been demonstrated. However, due to the vertical device layout, the vertical NW array-based transistors are challenging to fabricate and have huge parasitic capacitance which degrades their speed performance [84-86]. Making arrays of III-V NWs in-plane with the substrate is preferable for easy fabrication and better performance. However, so far, RF performance was reported only by detaching and aligning vertical NWs in a planar transistor layout [87, 88].

With the capability of growing site-controlled planar NWs (Chapter 5), we successfully developed a planar NW array-based HEMT structure for large-scale application. The growth is illustrated in Figure 6.1. Arrays of Au seeds (disk-like) with diameters ~ 150 nm, height ~ 30 nm and center-to-center separation ~ 300 nm were patterned on (100) SI GaAs substrates by EBL,

metal evaporation and liftoff processes (Figure 6.1a). The patterned sample was loaded into an Aixtron 200 MOCVD reactor for the growth. Undoped planar GaAs NW arrays were grown for 3 minutes under atmospheric pressure using the two-temperature-step ($450 \rightarrow 430$ °C) VLS growth method detailed in Chapter 3 (Figure 6.1b). Then thin films of a 3-nm undoped $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ spacer, a 50-nm Si-doped ($3 \times 10^{18} \text{ cm}^{-3}$) $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ top barrier and a 50-nm n^+ ($5 \times 10^{18} \text{ cm}^{-3}$) GaAs ohmic contact layer were successively deposited on the planar GaAs NW arrays under reactor pressure of 100 mbar using the two-temperature-step thin-film growth method ($500 \rightarrow 680$ °C) detailed in Chapter 3 (Figure 6.1c).

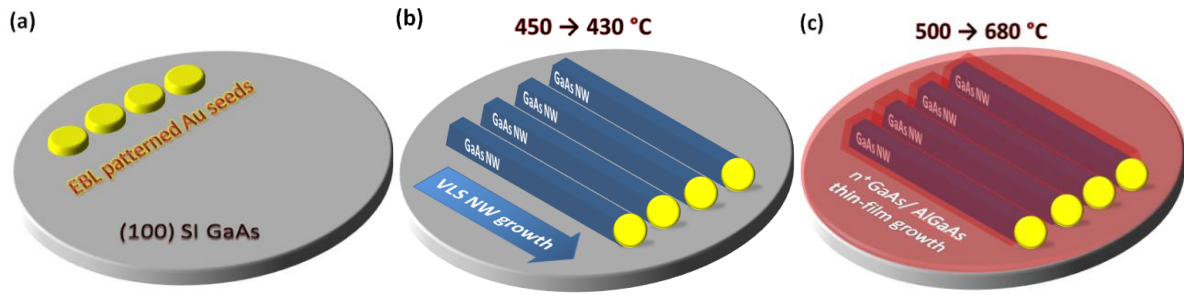


Figure 6.1: Illustration of the growth of the planar NW array-based HEMT structure. (a) Patterning of Au seeds. (b) VLS growth of planar GaAs NW arrays under atmospheric pressure and at $450 \rightarrow 430$ °C. (c) Conformal thin-film growth of the $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ spacer, $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ top barrier and GaAs ohmic contact layer under 100 mbar and at $500 \rightarrow 680$ °C. See Chapter 3 for the details of the growth conditions and Chapter 5 for the details of the EBL patterning technique.

In order to reveal the quality of the planar NW arrays embedded in the NW HEMT heterostructures, a control sample was grown experiencing only the VLS growth. The as-grown planar NW arrays have length over $30 \mu\text{m}$, indicating an axial NW growth rate (R_{axial}) of $>10 \mu\text{m}/\text{min}$. Figure 6.2a shows the top-view SEM image of the near-tip portion of a planar GaAs NW array on the control sample. The zoom-in top-view SEM image of the same NW array is also shown in Figure 6.2b. As can be seen, the lateral dimensions of the NWs are extremely

uniform along the same NWs and among different NWs. By inspecting the complete NWs, an average tapering factor ($R_{\text{axial}}/R_{\text{axial}}$, as defined in Chapter 3) of only 0.476 nm/ μm was extracted. Figure 6.2c is the cross-section SEM image of a cleaved planar NW array on the same sample. The planar NWs have isosceles-trapezoidal radial cross-section with perfect (111)A sidewall facets and (100) top facet.

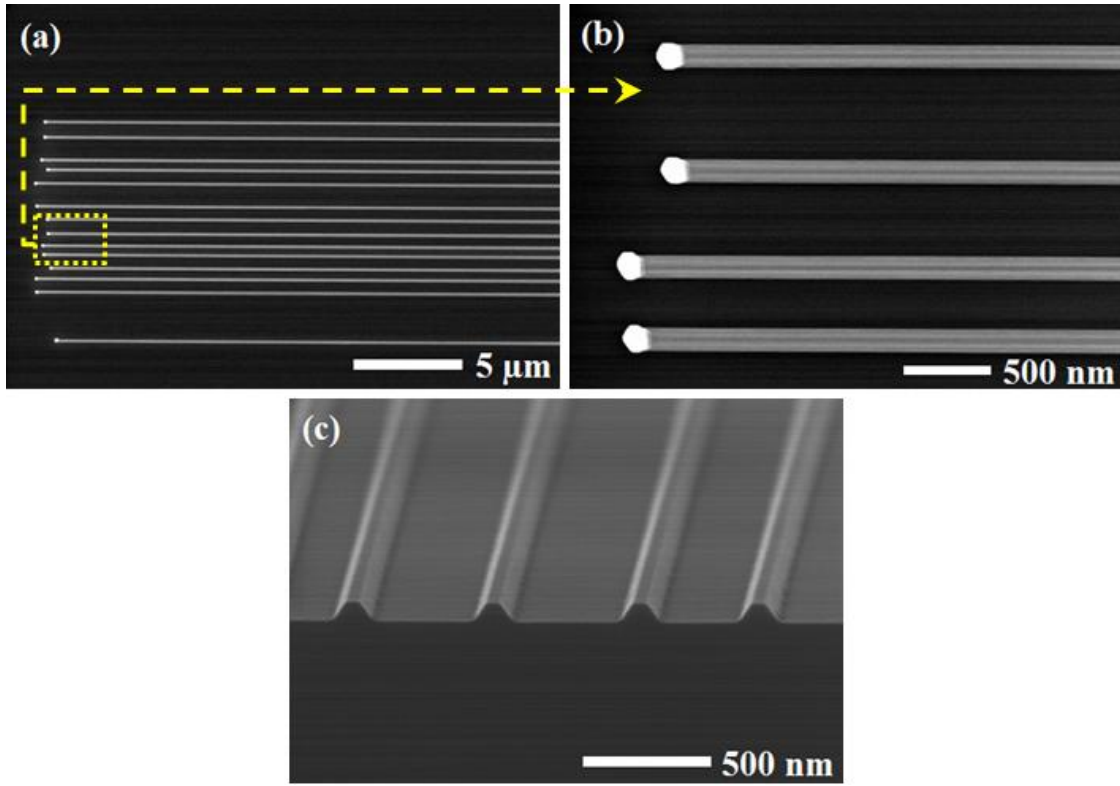


Figure 6.2: Images of as-grown planar GaAs NW arrays. (a) Top-view SEM image of the near-tip portion. (b) Zoom-in top-view SEM image. (c) Cross-section-view SEM image of a cleaved planar NW array on the same sample. The planar NWs have isosceles-trapezoidal radial cross-section with perfect (111)A sidewall facets and (100) top facet.

Figure 6.3a-b are the schematic and the cross-section SEM images of the planar NW HEMT heterostructure. $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ was selectively etched by diluted HF to reveal contrast. As can be

seen, the $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ barrier on the NW sidewalls is thicker than on the NW top facet, probably due to higher thin-film growth rate of the (111)A surfaces than (100) surfaces.

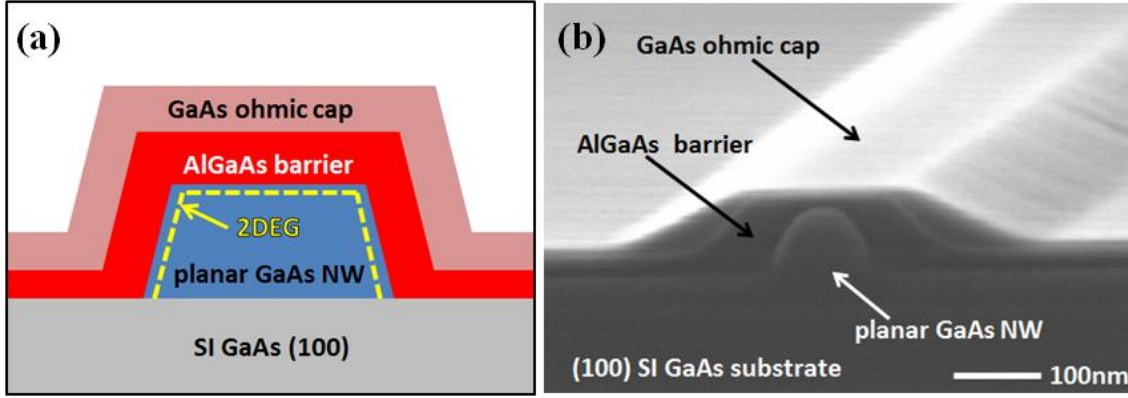


Figure 6.3: Schematic (a) and cross-section SEM image (b) of the planar NW HEMT heterostructure. $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ was selectively etched by diluted HF to reveal contrast.

6.2 Fabrication of planar NW array-based HEMT

The planar NW array-based HEMTs are fully-compatible with the conventional planar-processing. After the growth, ohmic contacts with 3- μm source-to-drain separations (L_{s-d}) were formed using a Ni/Ge/Au/Ni/Au metal stack alloyed at 400 $^{\circ}\text{C}$ in H_2 ambient for 30 seconds followed by ~ 200 nm deep wet-etch mesa isolation in acid and Ti/Au interconnect pad metal. Finally, centered Ti/Pt/Au T-gates with L_g ranging from 150 to 300 nm were deposited using EBL after a gate recess wet-etch step to remove the n^+ GaAs cap below the gate. The planar NW array-based HEMTs have a two-finger gate RF probe (ground-signal-ground) layout with planar GaAs NW arrays spanning across the double gate fingers as the channel. Figure 6.4a shows a tilt-view SEM image of a fully-processed planar NW array-based HEMT with 25 NWs and $L_g = 150$ nm. The magnification of the channel region is shown in Figure 6.4b. The ungated region appears merged because the shared GaAs ohmic contact layer smoothed the densely-packed

AlGaAs/GaAs-NW structures. However, the morphology of the AlGaAs/GaAs-NW structures can be seen in the center of the T-gate where the GaAs ohmic contact layer was selectively removed.

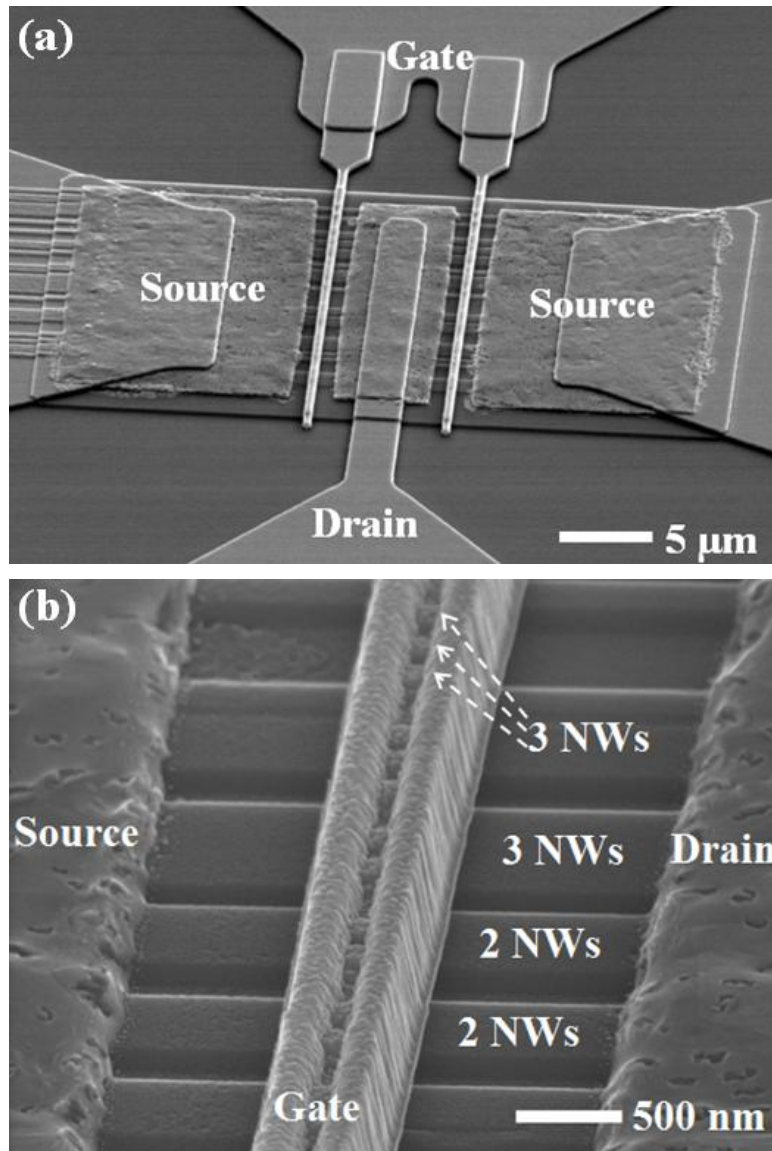


Figure 6.4: (a) Tilt-view SEM image of a fully-processed planar NW array-based HEMT with 25 NWs and $L_g = 150$ nm. (b) Zoom-in SEM image of the channel region. The morphology of the AlGaAs/GaAs-NW structures can be seen in the center of the T-gate where the GaAs ohmic contact layer was selectively removed.

6.3 DC characteristics of planar NW array-based HEMT

Our planar-NW HEMT technology allowed for conventional planar-processing and full-wafer automated DC/RF characterization. The DC characteristics of the planar NW array-based HEMT with 30 NWs spanning across the double gate fingers and $L_g = 150$ nm (as shown in Figure 6.4) are plotted in Figure 6.5a-c. Current normalization was done using the effective conducting width per NW of 210 nm (sidewall facet ~ 75 nm, top facet ~ 60 nm). Thus, the effective device width is $12.6 \mu\text{m}$ ($2 \times 30 \times 0.21 \mu\text{m}$). The output characteristics in Figure 6.5a were measured for V_{gs} from -0.6 to 0.6 V in steps of 0.2 V, and show excellent saturation at low V_{ds} . Figure 6.5b plots the normalized transfer characteristics for V_{ds} from 0.5 to 3 V in steps of 0.5 V. At $V_{ds} = 2$ V, the peak G_{m-ext} is $329 \mu\text{S}/\mu\text{m}$ and I_{d-max} is $225 \mu\text{A}/\mu\text{m}$. The extracted V_T is ~ 0.2 V, indicating enhancement-mode operation. Excellent $I_{on}/I_{off} \sim 10^4$, $SS \sim 102$ mV/dec and $DIBL \sim 151$ mV/V can be extracted from the semi-log transfer characteristics shown in Figure 6.5c. As can be seen, there are two distinct regions from I_{off} to I_{on} , due to possible earlier turn-on of the sidewall facets than the top facet as a result of slightly different barrier thicknesses (Figure 6.3b). Figure 6.3d shows the transfer characteristics of four devices with different L_g measured under the same condition. The V_T and peak G_{m-ext} conditions are the same for all four devices, which indicates excellent electrostatic gate control.

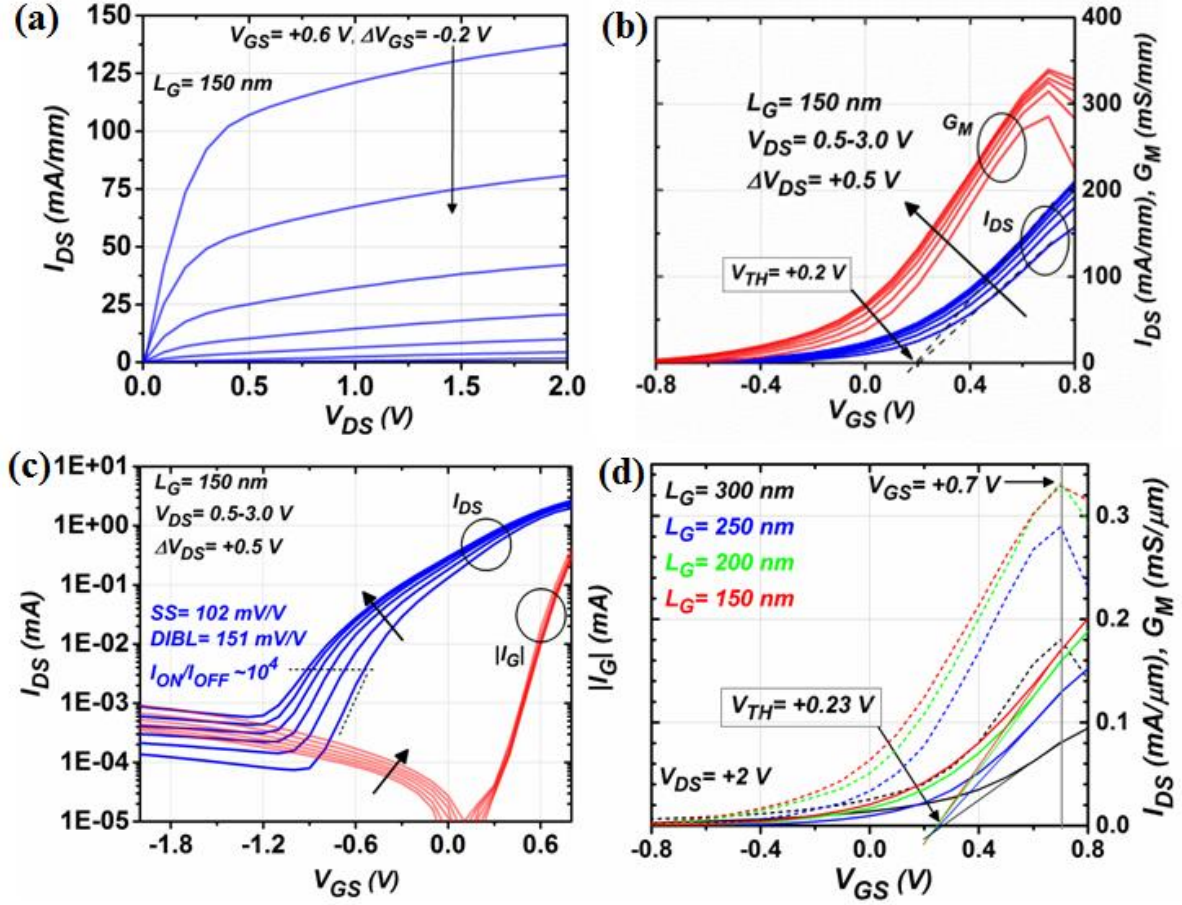


Figure 6.5: DC characteristics of a planar NW array-based HEMT with 30 NWs spanning across the double gate fingers and $L_g = 150$ nm (as shown in Figure 6.4). (a) Output characteristics for V_{GS} from -0.6 to 0.6 V in steps of 0.2 V. (b) Normalized transfer characteristics for V_{DS} from 0.5 to 3 V in steps of 0.5 V. (c) Transfer characteristics in semi-log form. (d) Transfer characteristics of four devices with different L_g with the same V_T and peak G_{m-ext} conditions.

A mesa-only device without any NWs in the channel was fabricated and tested on the same chip of the planar NW array-based HEMTs. The structure of the mesa-only device is the same as the thin-film regions among NWs in NW array-based HEMTs: below the Schottky T-gate there are 15-nm $Al_{0.33}Ga_{0.67}As$ barrier, 10-nm parasitic GaAs film channel (deposited during the VLS NW growth) and the SI GaAs substrate (see Figure 6.3b). Figure 6.6a shows the mesa-only device which has a single-channel with mesa width ~ 20 μ m, $L_g = 250$ nm and $L_{s-d} = 3$ μ m. Figure 6.6b plots the DC transfer characteristics of the mesa-only device in comparison with a

double-gate NW array-based HEMT with 25 planar GaAs NWs spanning across the double gate fingers. The NW array-based HEMT has the same mesa width, L_g and L_{s-d} as the mesa-only device. As can be seen, both the channel current (I_{ds}) and gate leakage current ($|I_g|$) of the mesa-only device are orders of magnitude below the current levels of the NW array-based HEMT, which indicates that the parasitic GaAs film deposited during the VLS GaAs NW growth is not conductive and does not contribute to the conductance of the NW HEMTs. The reason for the low conductance of the 10-nm parasitic GaAs film is the depletion caused by the pinned interface between the parasitic GaAs film and the SI GaAs substrate [89].

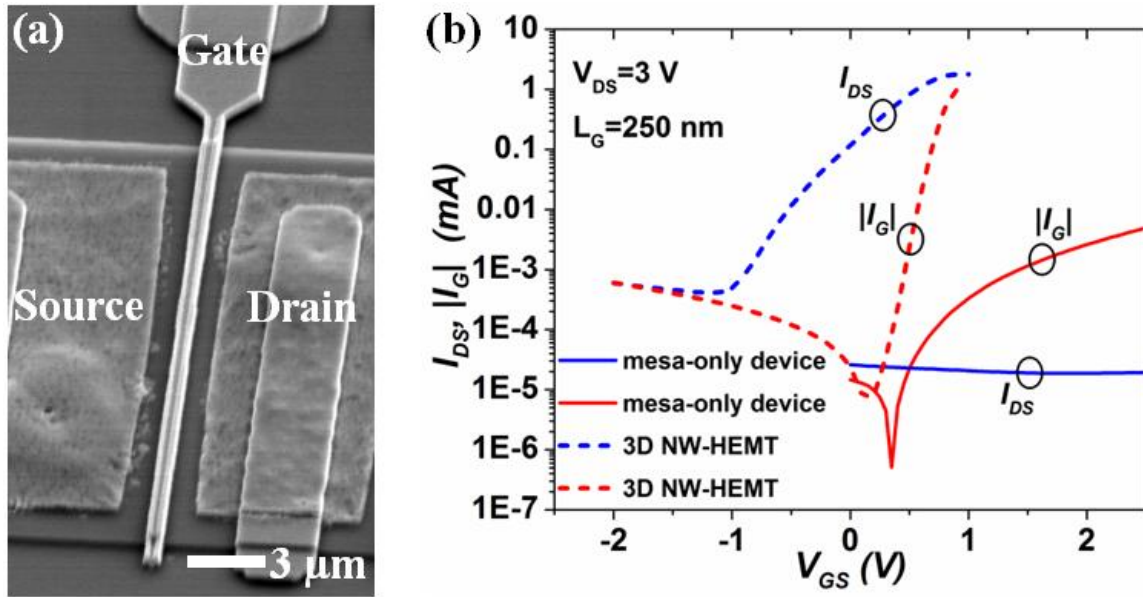


Figure 6.6: (a) Tilt-view SEM image of a single-channel mesa-only device with no NWs in the channel (mesa width $\sim 20\text{-}\mu\text{m}$, $L_g = 250$ nm and $L_{s-d} = 3\text{ }\mu\text{m}$). (b) DC transfer characteristics of the mesa-only device in comparison with a double-gate NW array-based HEMT with 25 planar GaAs NWs spanning across the double gate fingers.

6.4 RF characteristics of planar NW array-based HEMT

Small-signal RF gain measurements were performed using an automated system consisting of an Agilent E8364B parametric network analyzer with Cascade probes in the 1-40 GHz range at -27 dBm. Figure 6.7 shows the actual planar NW array-based HEMT chip under test. Calibration to the probe tips was accomplished using conventional off-chip short-open-load calibration. The cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) were determined by measuring where the current gain (H21) and maximum available gain (MAG) fall to unity with a -20 dB/dec slope versus frequency. To reveal the intrinsic performance, careful de-embedding of the pad capacitance was achieved by measuring the S-parameters of an open and short device with identical pad layout.

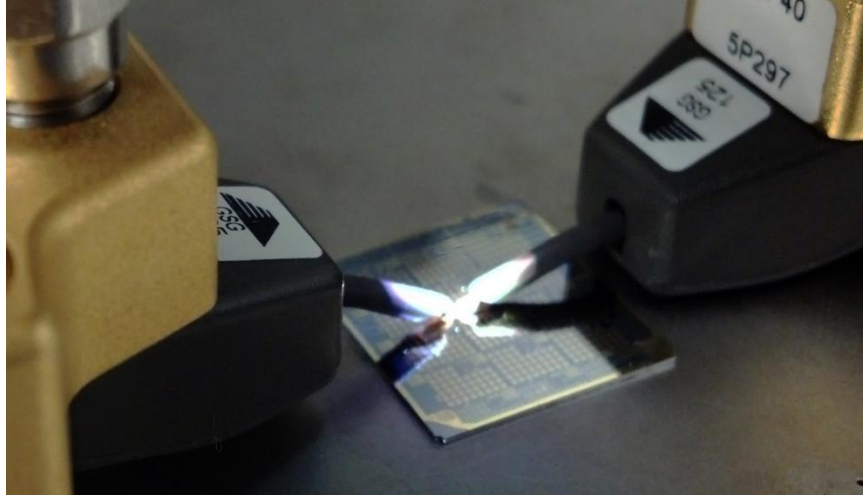


Figure 6.7: The planar NW array-based HEMT chip under RF small-signal measurement.

Planar NW array-based HEMTs with different gate length were measured in a wide bias range of $V_{gs} = 0-0.8$ V and $V_{ds} = 0.5-3.5$ V. The small-signal gain versus frequency of representative devices are shown in Figure 6.8a at $V_{gs}/V_{ds} = 0.6/2$ V. Both the f_T and f_{max} scale inversely with the L_g . Therefore, the best frequency response was from the device with $L_g = 150$

nm with $f_T/f_{\max} \sim 33/75$ GHz. The SEM images and DC characteristics of this specific device have been shown previously in Figure 6.4 and Figure 6.5. Figure 6.8b,c are the contour plots of f_T and f_{\max} of the same device ($L_g = 150$ nm) with respect to the V_{gs} and V_{ds} . Note that when both the V_{gs} and V_{ds} are less than 1 V, f_T/f_{\max} of $\sim 37/67$ GHz can still be achieved, which indicates the potential of our planar NW array-based HEMTs for low-power application.

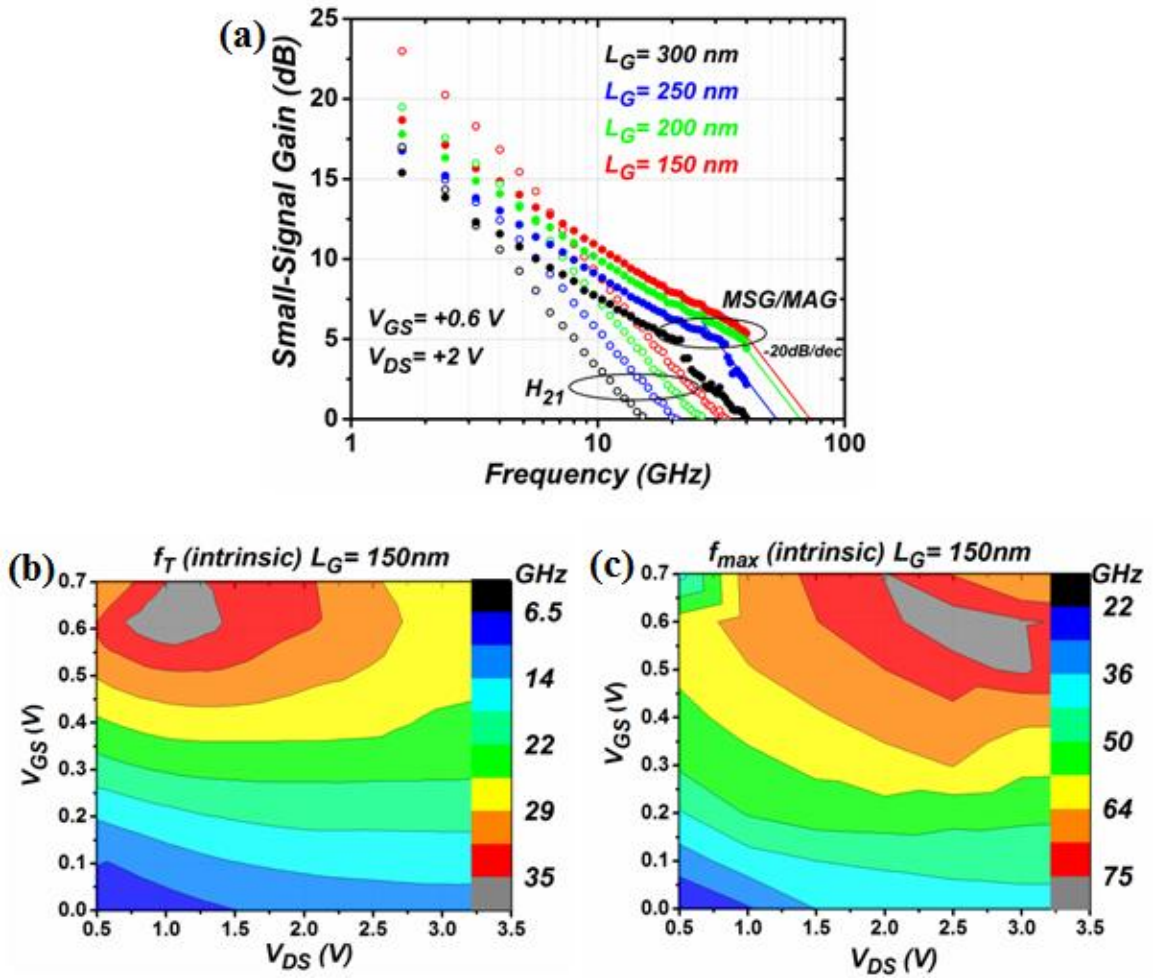


Figure 6.8: RF response of planar NW array-based HEMTs. (a) Small-signal gain versus frequency of representative devices with different gate length at $V_{gs} = 0.6$ V and $V_{ds} = 2.0$ V. Contour plot of (b) f_T and (c) f_{\max} with respect to V_{gs} and V_{ds} for the device with $L_g = 150$ nm characterized in (a).

A conventional small-signal equivalent circuit model of FETs as illustrated in Figure 6.9 was used to analyze the planar NW array-based HEMTs. The extrinsic elements L_{gate} , R_g , C_{pg} , L_s , R_s , L_d , R_d and C_{pd} are independent of the biasing conditions and can be determined by measuring the devices under cold, unbiased, and hot-FET conditions [90-92]. With the knowledge of the extrinsic elements, the intrinsic elements G_m , G_d , C_{gs} , C_{gd} , C_{ds} , R_i and τ can be directly extracted for any operational biasing. Table 6.1 lists the extracted device parameters of the planar NW array-based HEMT with $L_g = 150$ nm shown in Figure 6.8a at $V_{gs} = 0.6$ V and $V_{ds} = 1, 2$ and 3 V. The simulated 1-40GHz S-parameters with the extracted parameters at $V_{gs}/V_{ds} = 0.6/2$ V of the same device were plotted in Figure 6.10 and compared with the measurement. The model has excellent agreement with the measurement and is feasible for further analysis.

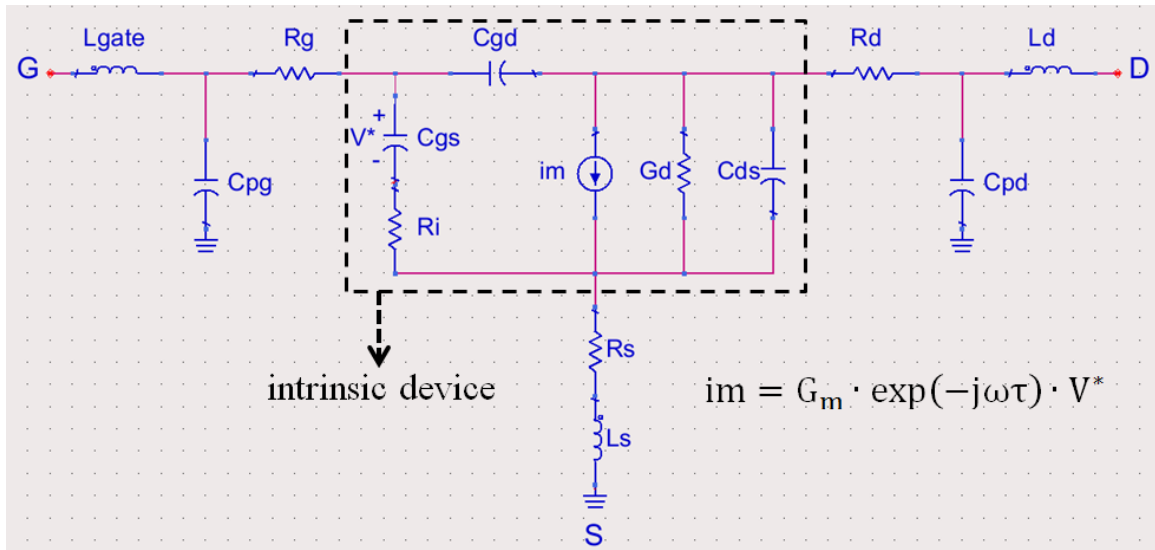


Figure 6.9: Conventional small-signal equivalent circuit model of FETs used in the analysis of the planar NW array-based HEMTs.

Table 6.1: Extracted device parameters of the planar NW array-based HEMT with $L_g = 150$ nm shown in Figure 6.8a at $V_{gs} = 0.6$ V and $V_{ds} = 1, 2$ and 3 V.

Parameters \ V_{ds}	1 V	2 V	3 V
C_{gs} (fF)	19.24	23.33	27.50
C_{gd} (fF)	11.68	10.06	8.92
C_{ds} (fF)	14.14	13.81	13.44
G_m (mS)	5.92	5.93	5.66
G_d (mS)	0.44	0.30	0.22
R_i (Ω)	25.80	15.72	15.75
R_{gd} (Ω)	7.26	36.54	70.57
R_s (Ω)	24.33	24.33	24.33
R_d (Ω)	33.49	33.49	33.49
R_g (Ω)	15.63	15.63	15.63

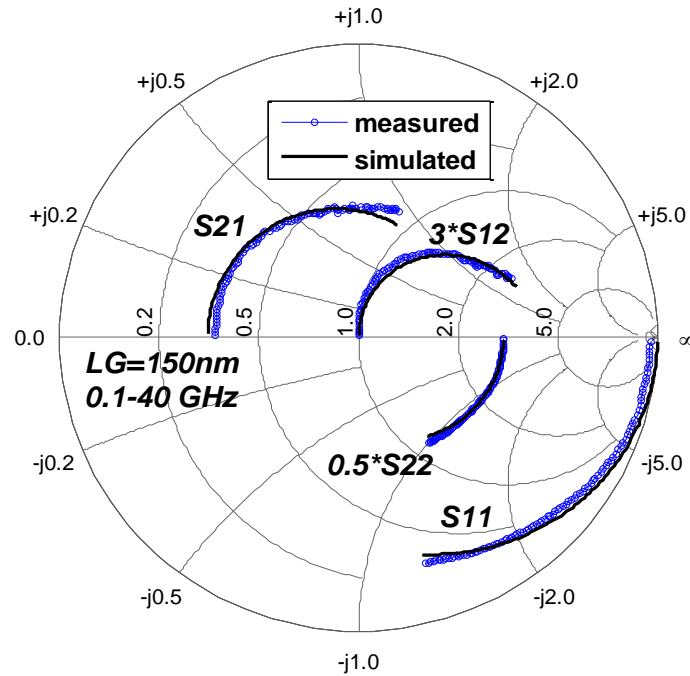


Figure 6.10: Simulated 1-40GHz S-parameters with the extracted parameters at $V_{gs}/V_{ds} = 0.6/2$ V of the planar NW array-based HEMT with $L_g = 150$ nm in comparison with the measurement.

Dividing the extracted G_m in Table 6.1 by the effective device width ($\sim 12.6 \mu m$) gives the scaled intrinsic transconductance G_{m_int} . The intrinsic electron velocity (v_{eff}) can be estimated by G_{m_int}/C_{diel} , where the C_{diel} is the intrinsic unit-area gate-to-channel capacitance [77, 78]. As illustrated in Figure 6.3b, the dielectric, namely the $Al_{0.33}Ga_{0.67}As$ barrier on the NWs, has different thickness on NWs' sidewall and top facets. The v_{eff} extraction steps of the NW array-based HEMT with $L_g = 150 \text{ nm}$ were shown in Figure 6.11. The v_{eff} for $V_{ds} = 1, 2$ and 3 V at $V_{gs} = 0.6 \text{ V}$ was calculated as $1.49 \cdot 10^7$, $1.49 \cdot 10^7$ and $1.42 \cdot 10^7 \text{ cm/sec}$, respectively. The lower v_{eff} at high $V_{ds} = 3 \text{ V}$ is due to the hot electron effect which would induce electrons in the low-mobility $Al_{0.33}Ga_{0.67}As$ barrier and degrade the electron velocity.

$G_{m_int} = \begin{matrix} 469.8 \\ \{ 470.6 \} \text{ mS/mm} \\ 449.2 \end{matrix}$	extracted from small signal model for $V_{DS}=1,2,3 \text{ V}$
$W_{NW} = 75 + 75 + 60 = 210 \text{ nm}$	effective width per NW
$\epsilon_{AlGaAs} = 13.1 \cdot \epsilon_0 \approx 1.16 \cdot 10^{-10} \text{ F/m}$	permittivity of $Al_{0.33}Ga_{0.67}As$ barrier
$d_{AlGaAs-side} = 50 \text{ nm}$	$Al_{0.33}Ga_{0.67}As$ barrier thickness on NW's sidewall facet
$d_{AlGaAs-top} = 11 \text{ nm}$	$Al_{0.33}Ga_{0.67}As$ barrier thickness on NW's top facet
$\epsilon_{GaAs} = 12.9 \cdot \epsilon_0 \approx 1.14 \cdot 10^{-10} \text{ F/m}$	permittivity of GaAs NW channel
$\Delta d = 8 \text{ nm}$	Distance of electron wave function's peak position to the AlGaAs/GaAs interface
$C_{diel-side} = \frac{\epsilon_{AlGaAs}}{d_{AlGaAs-side} + \Delta d \times \frac{\epsilon_{AlGaAs}}{\epsilon_{GaAs}}} = 2.00 \cdot 10^{-3} \text{ F/m}^2$	capacitance at NW's sidewall
$C_{diel-top} = \frac{\epsilon_{AlGaAs}}{d_{AlGaAs-top} + \Delta d \times \frac{\epsilon_{AlGaAs}}{\epsilon_{GaAs}}} = 6.07 \cdot 10^{-3} \text{ F/m}^2$	capacitance at NW's top facet
$C_{diel} = \frac{C_{diel-side} \times 2 \times 75 + C_{diel-top} \times 60}{W_{NW}} = 3.16 \cdot 10^{-3} \text{ F/m}^2$	effective intrinsic capacitance
$v_{eff} = \frac{G_{m_int}}{C_{diel}} = \begin{matrix} 1.49 \cdot 10^7 \\ \{ 1.49 \cdot 10^7 \} \text{ cm/sec} \\ 1.42 \cdot 10^7 \end{matrix}$	intrinsic electron velocity for $V_{DS}=1,2,3 \text{ V}$

Figure 6.11: The extraction of the v_{eff} of NW array-based HEMT with $L_g = 150 \text{ nm}$.

Based on the extracted v_{eff} , the intrinsic cutoff frequency $f_{T-\text{int}} = v_{\text{eff}}/(2\pi \cdot L_g)$ at $V_{gs}/V_{ds} = 0.6/1$ V is 158GHz ($\sim 5\times$ the measured value). The extrinsic f_T and f_{max} can be expressed as

$$f_T = \frac{G_m}{2\pi \left((C_{gs} + C_{gd}) \left(1 + \frac{R_s + R_d}{G_d} \right) + C_{gd} G_m (R_s + R_d) \right)} \approx \frac{G_m}{2\pi (C_{gs} + C_{gd})}, \quad (6.1)$$

$$f_{\text{max}} = \frac{f_T}{2\sqrt{G_d (R_g + R_i + R_s) + 2\pi f_T R_g C_{gd}}}, \quad (6.2)$$

where C_{gs} and C_{gd} are the gate-to-source and gate-to-drain capacitance, R_s and R_d are the source and drain access resistance, G_d is the output conductance, and R_g and R_i are the extrinsic and intrinsic gate resistance. The lower f_T/f_{max} we measured is primarily due to huge parasitic capacitance components in C_{gs} and C_{gd} . Since the intrinsic gate capacitance scales with the gate length, the parasitic components ($C_{gs,p}$ and $C_{gd,p}$) can be extrapolated as the y-intercept in the C_{gs} and C_{gd} versus L_g plots. Indeed, the extrapolation shown in Figure 6.12a indicates that 47% of the total gate capacitance ($C_{gs} + C_{gd}$) for the device with $L_g = 150$ nm is parasitic-related. Removing the parasitic components ($C_{gs,p}$ and $C_{gd,p}$) from the total gate capacitance, the f_T/f_{max} of the planar NW array-based HEMT with $L_g = 150$ nm can reach $\sim 49/110$ GHz as shown in Figure 6.12b. In order to mitigate the unwanted effect of parasitic capacitance on devices' RF performance, the ratio of parasitic capacitance to the total gate capacitance needs to be reduced. This can be done by down-scaling the thickness of the $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ barrier and optimizing the pitch of planar GaAs NWs in the channel.

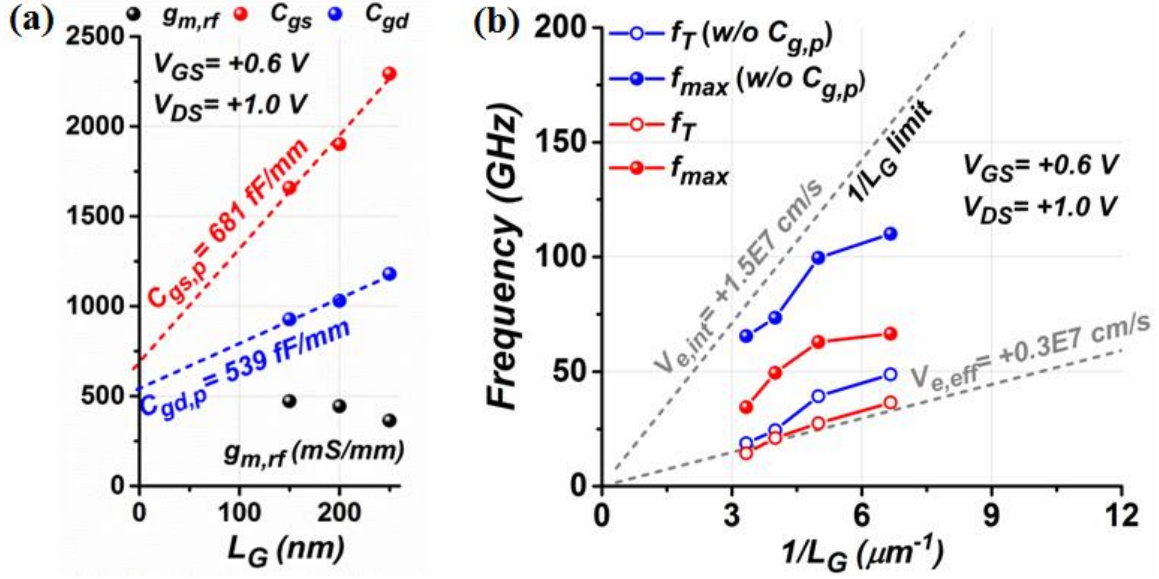


Figure 6.12: (a) Extrapolation of $C_{gs,p}$ and $C_{gd,p}$. (b) f_T and f_{max} versus $1/L_g$ of planar NW array-based HEMTs as shown in Figure 6.8a.

Figure 6.13 benchmarks our planar NW array-based HEMTs against the state-of-the-art nanoscale devices that have reported high-speed performance [84, 86, 87, 93-96]. The figures-of-merit (FoM) of both the RF and DC performance, $\sqrt{f_T f_{max}}$ and I_{on}/I_{off} , are plotted. Although using the relatively lower mobility channel material, our planar NW array-based HEMTs rank among the best for low-power RF and digital applications. With further optimization such as barrier down-scaling, incorporation of indium in the channel and employment of high-k gate dielectric, we fully expect >500 GHz RF performance to be achieved via our planar-NW FET technology.

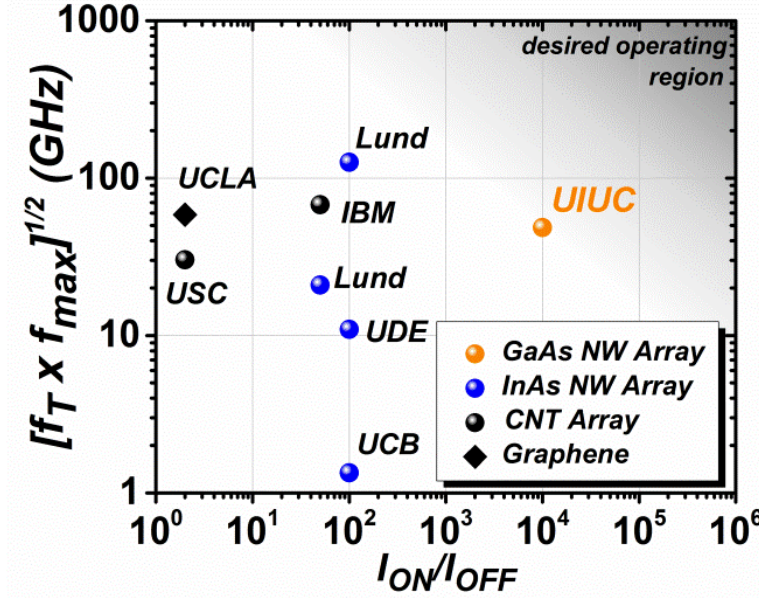


Figure 6.13: The RF and DC performance benchmark of the state-of-the-art nanoscale devices.

In summary, we have reported on the DC and RF characterization of the first planar NW array-based HEMTs through a bottom-up method. Our planar-NW technology enables monolithic 3D wrap-style transistor structure without top-down process-related damage. The global positioning of NWs in wafer-scale is through EBL patterning of Au seeds. The precise control of NW size, direction, and density, combined with compatible planar processing method, makes this versatile planar-NW FET technology well-postured for future low-power logic and RF applications.

CHAPTER 7 – FUTURE WORK

The demonstrated bottom-up planar NW array-based HEMTs have RF performance f_T/f_{\max} ~33/75 GHz from devices with gate length ~150 nm. To our knowledge, the achieved f_{\max} is the highest for any nanoscale device with VLS NWs, carbon nanotubes, or 2D sheets aligned in-plane with the substrate. Although impressive, we found there is still large room for improvement. Other potential applications of our planar-NW technology such as planar NW MOS HEMTs and planar NW FETs on flexible substrates shall also be explored in the near future.

7.1 Gate engineering for barrier thickness and leakage control

The current version of planar NW array-based HEMTs has 50-nm thick $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ barrier while the state-of-the-art InGaAs quantum-well HEMTs have barrier thickness of less than 10 nm [79]. Thick barrier renders small gate-to-channel capacitance and makes the devices' RF performance largely degraded by parasitic gate capacitance. Therefore, down-scaling the $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ barrier improves not only the DC but also the RF performances of the NW HEMTs. However, with the same bulk doping, thinner $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ barrier gives higher V_T which causes $G_{m-\text{ext}}$ and $I_{d-\text{max}}$ to be limited by the Schottky gate leakage. Adopting delta-doping rather than bulk doping in the $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ barrier can provide the same V_T with a thinner barrier (Figure 7.1). Delta-doped $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ barrier also facilitates electron transfer from the barrier to the channel, which would improve the $G_{m-\text{ext}}$.

One of the unique challenges about forming a highly delta-doped barrier layer for the NW channel is the multi-faceted surface profile of NWs. In the case of planar GaAs NWs on (100)

GaAs substrates, the NW surfaces are (100) on top and (111)A on the sidewalls. Because of the different crystal orientations, doping uniformity and saturation points need to be studied systematically.

As can be noticed in devices' DC transfer curves, the off-state current of planar NW HEMTs is governed by the leakage current from the reverse-biased Schottky gate diode. The I_{d-max} is also limited by the leakage current from the forward-biased Schottky gate diode. In order to make planar-NW FETs feasible for digital application, the gate leakages need to be suppressed for high I_{on}/I_{off} . Thus, a planar-NW MOS HEMT structure is desired. A planar-NW MOS HEMT, as illustrated in Figure 7.1, can be fabricated by adding a high-k dielectric layer between the gate metal and the AlGaAs barrier after surface passivation. Surface passivation can be achieved by immersing the samples in 29% $(NH_4)_2S$ solution [97].

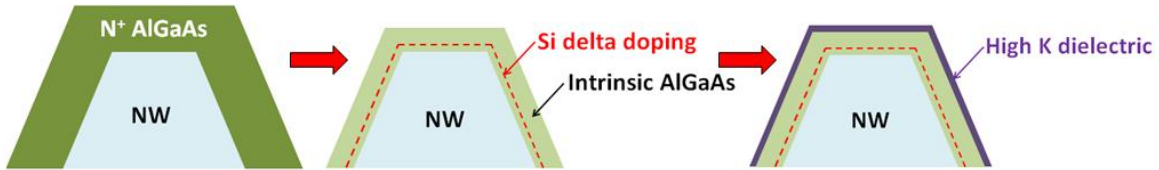


Figure 7.1: AlGaAs barrier thickness scaling and high-k dielectric addition for low-power high-speed planar-NW FETs.

We propose two process flows for fabricating planar NW MOS-HEMTs: ‘S/D first’ and ‘high-k first’. As illustrated in Figure 7.2a, the ‘S/D first’ process directly inserts the surface passivation and ALD Al_2O_3 steps right after the gate recess etch step in the process flow of planar-NW HEMTs. Because the existing alloy S/D cannot endure high temperature (600 °C) process, the post ALD annealing step to improve the ALD Al_2O_3 quality is omitted. However, in the ‘high-k first’ process, since the ALD Al_2O_3 would be done before the alloy S/D, the post ALD annealing can be added (Figure 7.2b).

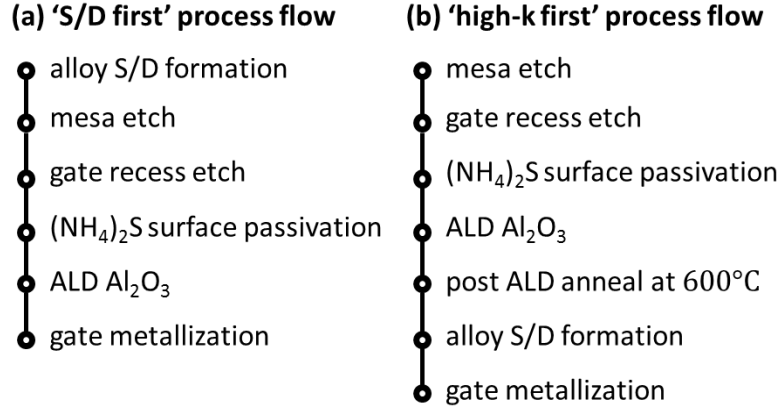


Figure 7.2: (a) 'S/D first' and (b) 'high-k first' processing flow of planar-NW MOS HEMTs.

Preliminary NW MOS-HEMT results from the 'S/D first' process were obtained. The DC transfer characteristics of the NW MOS-HEMT are compared with a NW HEMT and shown in Figure 7.3. The two devices have the same AlGaAs/GaAs-NW heterostructure and have a single NW in the channel. The NW MOS-HEMT has 8-nm Al₂O₃ as the gate dielectric, $L_{s-d} = 5 \mu\text{m}$ and $L_g = 3 \mu\text{m}$ while the NW HEMT has no gate dielectric, $L_{s-d} = 5 \mu\text{m}$ and $L_g = 1 \mu\text{m}$. Because of the passivation of the gate region by sulfide and ALD Al₂O₃, the NW MOS-HEMT has ~ 1-V negative V_T shift compared with the NW-HEMT. However, with a longer gate, the NW MOS-HEMT has larger drive current than the NW HEMT. More noticeably, the forward and reverse bias gate leakage currents in the NW MOS-HEMT are seven and three orders of magnitude lower, respectively, than those in the NW HEMT, which proves the low-power potential of planar NW MOS-HEMTs. We expect better device performance of 'high-k first' NW MOS-HEMTs since the quality of ALD Al₂O₃ can be further improved by the post ALD annealing.

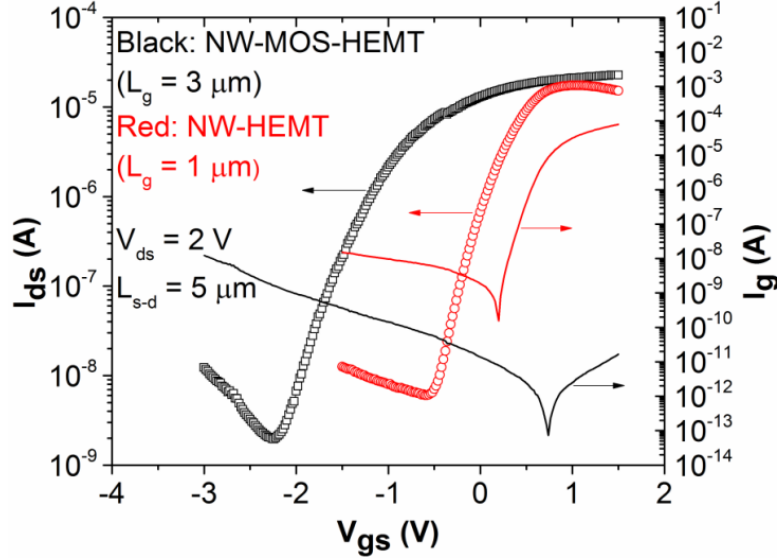


Figure 7.3 Transfer characteristics of single-NW channeled NW MOS-HEMT and NW HEMT. The NW MOS-HEMT has 8-nm Al_2O_3 as the gate dielectric, $L_{s-d} = 5 \mu\text{m}$ and $L_g = 3 \mu\text{m}$. The NW HEMT has no gate dielectric, $L_{s-d} = 5 \mu\text{m}$ and $L_g = 1 \mu\text{m}$.

7.2 Channel engineering

Using channel materials with higher electron mobility (thus higher electron saturation velocity), we can boost both the $I_{d-\text{max}}$ and $G_{m-\text{int}}$ of the planar-NW FETs. Since $G_{m-\text{int}}$ is proportional to the electron mobility, it is clear that replacing the channel with higher mobility III-V semiconductors such as InGaAs and InAs would yield significant improvements in speed [98]. Figure 7.4 shows two strategies we propose for this purpose: wrapping planar GaAs NWs with InGaAs QW and growing planar InGaAs (or InAs) NW channel on InP substrates. For the first strategy, the indium composition should not exceed 30% due to the lattice-mismatch problem. For the latter strategy, planar InGaAs NWs from the VLS growth may suffer from phase-segregation issues and InAs NWs can have large lattice-mismatch with the InP substrate.

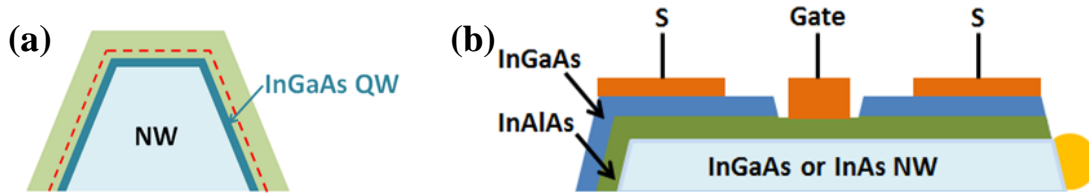


Figure 7.4: Channel engineering for high-speed application: (a) wrapping planar GaAs NWs with InGaAs QW and (b) growing planar InGaAs (or InAs) NW channel on InP substrates.

7.3 Flexible and wearable electronics

Flexible and wearable electronics have great potential for medical sensing, display and entertainment applications [99]. Most of today's flexible and wearable electronics are built by transfer-printing rigid Si-based devices to flexible substrates and then making interconnects on the flexible substrates. However, there is tradeoff of the flexibility of the electronics and the size of the transferred devices. The larger the transferred devices, the less flexible the built electronic circuits. Planar-NW FETs have the potential to resolve this problem since they are fabricated with a novel bottom-up process with full controllability of the size, density, and positioning of the discrete nanoscale components. Transfer-printing of planar NWs with great registration and alignment was demonstrated previously by our group [25]. With an integrated high aluminum content AlGaAs sacrificial layer, the active regions of the planar-NW FETs can be transferred by selectively undercutting the sacrificial AlGaAs with HF acid. Figure 7.5 illustrates the transferring process flow. Due to the discrete feature of the NW channel, the gaps among the NWs allow free bending of the flexible substrates without affecting the performance of the devices. Because of the 3D channel in planar-NW FETs, the interface between the transferred NWs and the substrate would not degrade the device performance. We expect flexible and wearable system-on-chip (SOC) circuits to be assembled using our planar-NW technology in the near future.

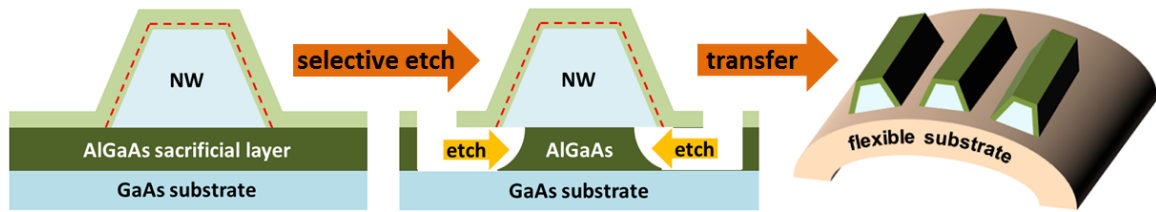


Figure 7.5: Transfer-printing planar-NW FETs with monolithic integrated AlGaAs sacrificial layer for flexible and wearable electronics.

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